Impact study of substrate materials on wireless sensor node RF performance

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Abstract

In this paper, the effect of the substrate on wireless sensor network (WSN) node's RF performance is studied experimentally by using different substrate materials with different thickness. A six-layer FR4 substrate PCB WSN node is fabricated and compared with the original two-layer FR4 PCB node to show the impact of substrate material thickness. Also a six-layer node with a flexible substrate demonstrates the different substrate effects with the FR4 substrate PCB. All these demonstrators are modeling by RF circuit analysis method and simulated in the Ansoft Designer software. Simulation results match the experimental measurement. An optimization method based on simulation for WSN node design with different substrate is presented. This analysis, modeling, simulation and optimization procedure can be carried out on some novel substrate materials such as LTCC and LCP.

Introduction

However, from RF system point of view, very little effort was done in considering these technologies as components which could change the final RF performance of the system. The aim of this paper is to develop a methodology to model the advanced packaging technologies for RF circuit simulation and obtain an optimized solution of the whole system. Statistical methods, like standard deviation, coefficient of variation, regression, curve fitting, are utilized during the parameter sweep procedure to get the optimization results.

In this paper, the impacts of a wide range of parameters on RF performance were studied and a statistical based method is proposed to improve the return loss. The paper is organized as the following:

- Main focus description: poor return loss caused by improper impedance matching.
- Modelling of the RF circuit, including the packaging and substrate.
- Description of the statistical methods used during analysis.
- Optimization performed to improve the return loss. Measurements were carried out to match the optimized solution.

System overview and the problem

The radio chip used in this paper is the high performance, ISM Band, FSK/ASK transceiver IC ADF7020. The wireless sensor node is also equipped with a MSP430 low power microcontroller, and an energy source.

An evaluation board of ADF7020 is provided by Analog Devices. Based on the reference design from the ADF7020 evaluation board datasheet, a credit card shape flat mote (named as "Tyndall mote" in this paper) with flip chip bare die of ADF7020 is developed with the same circuit connection.

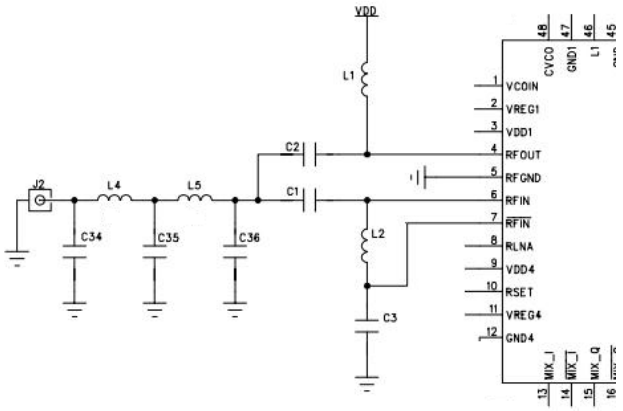

Figure 1. The balun circuit of the transceiver

The RF circuit, shown in Figure 1, between the ADF7020 chip and the antenna is critical to impedance matching. The RFIN and $\overline{\text{RFIN}}$ are the differential ports for receiving, while the RFOUT is for transmitting data. A balun circuit matches the chip ports with the SMA antenna connector J2. The balun consists of L1, L2, L4, L5, C1, C2, C3, C34, C35 and C36.

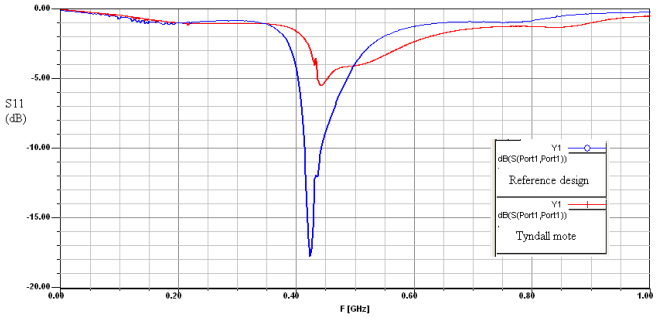

Figure 2.Return loss measurements of the two nodes

The working frequency of 433MHz for the ADF7020 transceiver was selected and measurements of S11 were carried out at the antenna SMA connector for the reference evaluation board and the Tyndall mote.

S11, also known as return loss, is the loss of signal power resulting from the reflection caused at a discontinuity in a transmission line. Smaller S11 means better circuit impedance matching and less power loss. Figure 2 illustrates that the reference design has a good impedance matching (around -20dB of return loss), while the other is behaving poor (only -5dB of return loss).

The modifications between the Tyndall mote to the reference design should be the reasons for the problem, including substrate thickness (6 layers PCB vs. 2 layers PCB), interconnect change (flip chip vs. packaged wire bonding) and the related PCB tracks.

In the following chapters, modelling, analysis and optimization were performed to provide a reliable method for the return loss optimization.

System overview and the problem

The model was based on the circuit shown in Figure 1, with some packaging and microstripline parameters added. To ensure the modelling being precise, all related parameters should be considered. These parameters included mainly the passive components, PCB layout details (track and layer stack-up) and RF ports characterization. The model and parameter values were imported into Ansoft Designer for simulation and analysis.

A. Passives

The discrete passives in Figure 1 can be modelled as ideal or real components, depending on the accuracy requirement. The real components have parasitic like ESR and ESL, which could be obtained from the manufacturer or Ansoft Designer vendor library. The pads of the surface mount components are treated as micro-stripe transmission lines.

B. PCB substrate

Not only the discrete components, but also the PCB tracks and substrate should be modelled. Figure 3 gives the schematic of the substrate and the micro-stripe line. All the PCB tracks are modelled as micro-stripe lines.

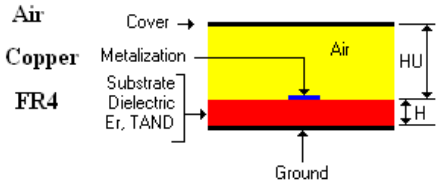

Figure 3. Schematic of the substrate stack-up

Parameter	Value
H	0.154mm
HU	100mm
εr (FR4)	4.5
tanδ	0.002
Copper thickness	35μm

Table 1. PCB and cover material properties

C. PCB tracks

Once the stack-up has been defined, individual transmission line sections are modelled by specifying the trace width and physical length of each section. Interconnect features such as corners and bends, whose effects can be significant at high frequencies, and are modelled for accuracy.

Special modelling of the following 50μm PCB tracks, in red colour in Figure 4, to the RF die ports was performed. These tracks play the same role of the wire-bonding to connect the die with the outside PCB. The width is as narrow as 50μ, while it is 0.25mm wide for the reference design (BGA packaging).

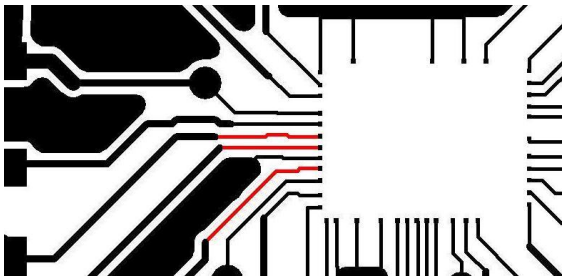

Figure 4. The 50μm width PCB tracks of the flip-chip interconnect

D. RF ports of the transceiver

The three RF ports are essential for modelling as passive components because it is difficult to simulate the circuit with some active components. The lumped element models of the ports, presented in Figure 5, are given by [6]. The values of the passive components are also listed in [6], or can be obtained by impedance measurements of the ports.

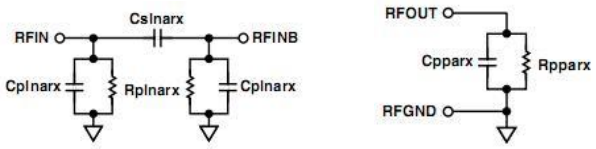

Figure 5. The LNA (left) and PA (right) models

E. Parameter sweep simulation

To show the idea of the proposed statistical analysis, there is no need to list and analysis all the huge amount of parameters. Instead, some parameters of different types are selected:

- Substrate related: dielectric constant and thickness of the substrate.
- Interconnect related: Interconnect track width, which differs from 0.25*mm* for the packaged chip to only 50μm for the flip-chip die.
- Passive components: C1 and C2 are selected as an example. Other parameters can be chosen as well.

Parameters	Reference value
Dielectric constant	4.5
Substrate thickness	0.154mm
Interconnect track width	0.25mm
C2	10nF
C1	4.7nF

Table 2. Reference values for the parameters

All the parameter values were all normalized by their reference design value, listed in Table 2. The return loss is showed by original value rather than in dB for analysis purpose.

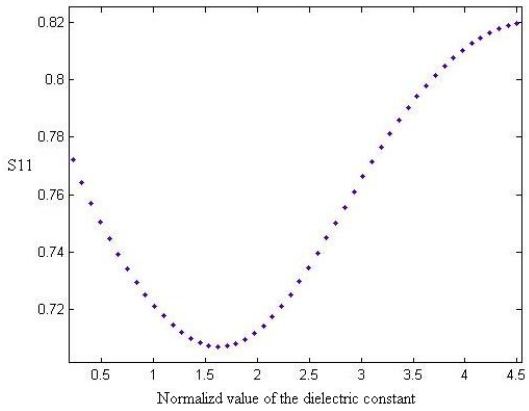

Figure 6. S11 simulation results for the dielectric constant sweep

Figure 6 shows an example of the parameter sweep simulation by Ansoft designer. The frequency is set at 433MHz. By sweeping the parameter value of the substrate dielectric constant, the corresponding return loss simulation results can be obtained.

System overview and the problem

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Following the optimization procedure proposed, sweep of passive components' values was performed to get an optimized return loss simulation result. The reason to sweep the passives is that replacing the passives with new values is much easier than replacing all other parameters.

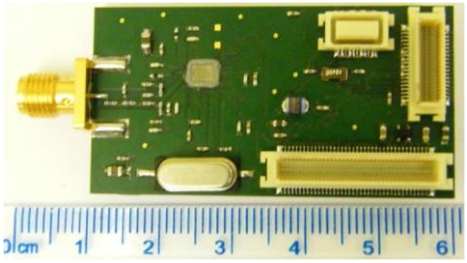

Figure 11. The wireless mote with a flip-chip bare die

Finally the new values of the passives were applied for PCB assembly. Measurements were compared with the simulation results until a good match was achieved. The optimization procedure was ended at this step.

In our case, optimization suggested changing the value of C2 from 10pF to 36pF and C1 from 4.7pF to 5.6pF. This change is to overcome the return loss degrade caused by substrate thickness change and layout impact of the flip-chip interconnect.

The measurement of return loss was carried out on the mote shown in Figure 11. The mote had an ADF7020 die flip-chip mounted on the left part of the board.

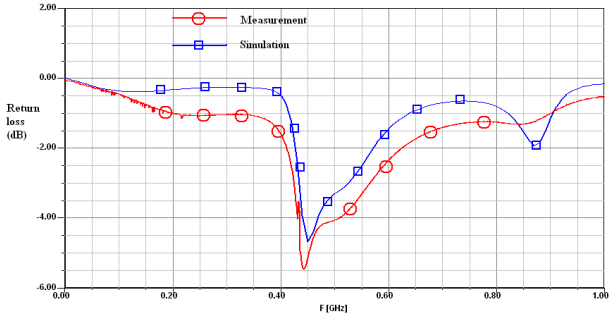

Figure 12. Simulation and measurement of the return loss with the recommended values of the passives

The result in Figure 12 partly explained the necessity to do simulation and optimization for the wireless mote using new interconnect technology or different substrate stack-up or PCB layout. There were lots of reasons about the poor return loss in Figure 12, including the substrate thickness change, the special requirement of the PCB layout for the bare die routing.

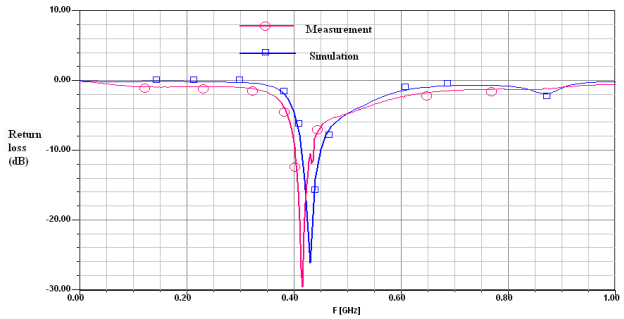

Figure 13. Simulation and measurement of the return loss with the optimized values of the passives

Simulation and measurement of the return loss, shown in Figure 13, were carried out again according to optimization solution. The return loss at 433MHz improved to -25dB for both simulation and measurement results (Figure 13). This level of return loss meant good impedance matching of the balun circuit. Finally Figure 14 illustrates that the return loss degrade was compensated with the help of new C1 and C2 values.

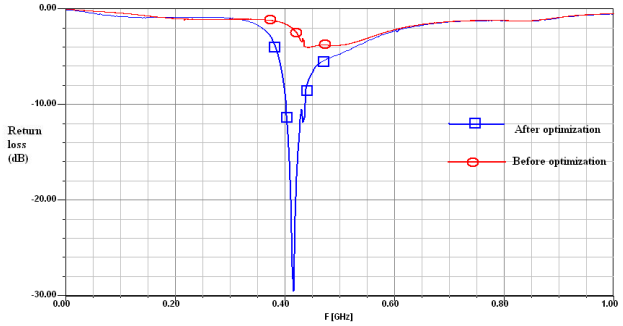

Figure 14. Measurements of the return loss
before and after optimization

$$c^2 = a^2 + b^2. \quad (1)$$

Conclusion

In this paper, the return loss of a wireless sensor node with a flip-chip bare die and more complex layer stack-up is compared with the reference transceiver board's return loss. Modeling counting on passive components, RF ports, substrate and interconnect parameters was developed and simulated by Ansoft Designer. Place conclusions here. Several statistical methods, including the coefficient of variation, regression and curve fitting, were applied to analysis and optimize the return loss impacts and behaviors. Then based on the regression functions got in the previous study, an extreme value search was carried out on the functions to get an optimized return loss (minimum). Measurements, before and after optimization, not only fit the Ansoft Designer simulation, but also showed a major improvement of the return loss from -5dB to -25dB.

Conclusion

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