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Authors	Wu, Xueyan;Kulkarni, Jaideep S.;Collins, Gillian;Petkov, Nikolay;Almecija, Dorothee;Boland, John J.;Erts, Donats;Holmes, Justin D.
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The Synthesis and Electrical and Mechanical Properties of Silicon and Germanium Nanowires

*Xueyan Wu[1,2], Jaideep S. Kulkarni[1,2], Gillian Collins[1,2], Nikolay Petkov[1,2], Dorothée Almécija[1,3], John J. Boland[1,3], Donats Erts[1,4] and Justin D. Holmes[1,2]**

[1]Centre for Research on Adaptive Nanostructures and Nanodevices (CRANN) Trinity College Dublin, Dublin 2, Ireland

[2]Department of Chemistry and the Tyndall National Institute, University College Cork, Cork, Ireland

[3]School of Chemistry, Trinity College Dublin, Dublin 2, Ireland

[4]Institute of Chemical Physics, University of Latvia, LV-1586 Riga, Latvia

* Author to whom correspondence should be addressed. E-mail: j.holmes@ucc.ie

Tel: +353 (0)21 4903608

Fax: +353 (0)21 4274097

Abstract

The development of semiconductor nanowires has recently been the focus of extensive research as these structures may play an important role in the next generation of nanoscale devices. Using semiconductor nanowires as building blocks, a number of high performance electronic devices have been fabricated. In this review, we discuss synthetic methodologies and electrical characteristics of Si, Ge and Ge/Si core/shell nanowires. In particular the fabrication and electrical properties of a variety of nanowire-based field effect transistors (FETs) are discussed. Although the bottom-up approach has the potential to go far beyond the limits of top-down technology, new techniques need to be developed to realize precise control of structural parameters, such as size uniformity, growth direction and dopant distribution within nanowires to produce nanowire-based electronics on a large scale.

1. Introduction

1 D semiconducting nanowires possess some very unique properties such as quantum confinement effects, surface sensitivity and low leakage currents which make them attractive as building blocks for functional nanosystems and next generation electronics. Chemically synthesized semiconductor nanowires have attracted much attention as key parameters, such as diameter, length, growth direction, chemical composition and doping levels can be rationally and predictably controlled during the synthesis process, which may enable their integration in a wide range of devices [1-6]. Semiconductor nanowires have been used for the assembly of FET devices with either a top, bottom or surround gate architecture [7-12]. Low-temperature bottom–up assembly methods offer unique opportunities and alternatives for the design and fabrication of single- and multi-nanowire device structures on a range of substrates without the need for lithography, which currently dominates many top-down technologies.

Si transistor technology, in particular CMOS, has played a pivotal role in allowing a decrease in feature sizes by a factor of 0.7 every 3 years as predicted by Moore's law [13]. Currently Intel has started production at the 45 nm technology node using an all dry process with other chipmakers in-step or close behind. However, to improve device performance, increase device density and reduce power consumption, further downscaling will be greatly desirable. Great attention has been paid to the 32 nm and 22 nm nodes although it is highly challenging according to the International Technology Roadmap for Semiconductors (ITRS):2007 [14]. ITRS 2007 expects that by 2018, the metal oxide semiconductor

field-effect transistor (MOSFETs) node will be scaled down to 18 nm and beyond, with the gate length down to 7 nm (Table 1). However planar bulk Si MOSFETs are unlikely to meet the ITRS roadmap requirements in the long-term and hence new structural, material and fabrication technology solutions, that are generally compatible with current and Si manufacturing, have to be exploited to maintain the historical CMOS performance trend.

Compared with bulk semiconductors, semiconductor nanowires have attracted considerable attention because of their unique electrical properties and intrinsically miniaturized dimensions [15-17]. Semiconductor nanowires can have an on/off current ratio which varies by many orders of magnitude for small changes in gate voltage. They also offer the possibility of ballistic transport since electron scattering in 1 D is much reduced [18]. In general, the performance characteristics of nanowire-based electronic devices often rivals devices constructed from the best bulk and epitaxial single-crystal semiconductors. Semiconductor nanowires are looked upon as a potential solution to some of the most daunting challenges in the painstaking effort to shrink CMOS FET devices deeply into the nanometre regime. Ge and Si nanowires offer a performance enhancement of FETs without jeopardizing device reliability. FETs based on boron and phosphorus-doped Si and Ge nanowires have been actively studied during the past several years as these two materials offer great compatibility with the industrial chip technology [18-22]. Devices based on Si and Ge nanowires display performances that are comparable to the best reported for corresponding planar devices.[23, 24]

In this article, we review the synthesis, electronic and mechanical properties of Si, Ge and

core/shell Ge/Si nanowires as well as the performance of nanowire-based FET devices.

2. Silicon Nanowires

2.1 Si Nanowire Synthesis

Various methods have been employed to synthesize Si nanowires including electron beam lithography [25], reactive ion etching [26] and laser ablation [27]. Among the lithography approaches, special attention should be given to the method developed by Heath and co-workers for depositing aligned arrays of Si nanowires by the supperlatice nanowire pattern transfer (SNAP) technique, since very small and uniform diameter structures were obtained[28]. Most Si nanowires have been synthesised by the classical metal catalyzed vapor-liquid-solid (VLS) growth process using gold nanoparticles as catalytic seeds. In the VLS process, the Si precursor decomposes on the surface of the catalyst and Si diffuses into the metal forming a liquid alloy. Upon reaching supersaturation, a Si nanowire is precipitated and the liquid alloy drop remains at the end of the nanowire as it grows in length [29]. The diameter of each Si nanowire is largely determined by the size of the catalyst particle and growth conditions. It has been demonstrated that Si nanowires with specific dimensions can be obtained by controlling the diameter of gold particles, which can be formed by metal deposition, photolithography, laser ablation, evaporation or nanocluster formation [8, 23, 24, 30-34]. The VLS process has also been used to grow doped Si nanowires using boron sources such as trimethylboron (TMB) and diborane (B_2H_6) [35]. At the specific growth conditions used, B-doped Si nanowires grown using B_2H_6 consisted of a crystalline core with a thick amorphous Si coating, while the B-doped Si nanowires grown from TMB were predominantly single crystalline even at high boron concentrations.

The authors suggested that the difference in the crystallinity can be attributed to the higher thermal stability and reduced reactivity of TMB compared to B_2H_6. Nevertheless a detailed mechanistic study is still necessary to uniquely identify the conditions responsible for the difference in the crystalinity of the doped Si nanowires obtained.

Nanoporous templates have been employed to synthesize Si nanowires. High-density, free-standing, vertical Si nanowires with well-defined diameter and spacing were synthesized by Lombardi *et al.* using a non-lithographic technique (Figure 1) [36]. An anodized aluminium oxide (AAO) membrane was first transferred onto a Si (111) substrate, followed by the evaporation of Au through the AAO pores. The AAO was then removed and Si nanowires were grown from the patterned substrate by the VLS technique. This method enables the fabrication of Si nanowires with a high packing density, up to 60 wires/μm^2 and is the highest reported density of vertical Si nanowires on a Si substrate without lithographic means. Additionally Redwing *et al.* have combined template-directed synthesis and VLS growth techniques to produced Si nanowires ranging from 45 to 200 nm [37-39]. These Si nanowires were single crystals with a [110], [111], or [100] growth direction, or bicrystalline containing a single (111) twin boundary along the [112] growth axis. It was noted that when longer reaction times were employed larger diameter nanowires grew on the surface of the membranes. The authors speculate that the size difference between these nanowires is likely due to a change in the shape of the Au tip from cylindrical to hemispherical, which occurs when the Au-Si liquid alloy is no longer constrained by the pore walls. Nevertheless a detailed investigation and observation of the Si nanowires within the AAO channels to assess loading factors and their distribution along

the length of the membrane was not discussed. Investigation of the Si nanowire growth characteristics showed that the length of the Si nanowires was linearly dependent on the growth time over a temperature range from 400 to 600 °C, and over a SiH_4 partial pressure range from 0.13 to 0.65 Torr. This approach also provided a method for contact formation as the AAO membrane could be used as a support structure based on the work by Erts *et al* [40].

2.2 Silicon Nanowire Field Effect Transistors

Lieber *et al* have been extremely successful in fabricating and electrical characterizing Si nanowire-based FET devices. They have demonstrated that carrier type (electrons, n-type; holes, p-type) and carrier concentrations in single-crystal Si nanowires can be controlled during the growth process using phosphorus and boron dopants [24]. Back-gated n-type FETs were fabricated based on p-doped 20 nm Si nanowires grown with a gold nanocluster mediated VLS technique. It was reported that these FETs have an electron mobility 100 times higher than those prepared in a laser-assisted catalytic growth process and are comparable to high-performance planar Si FETs. While investigating the electrical properties of P-doped devices with different dopant concentration, it was found that the transconductance values and mobility values decreased with decreasing dopant concentration, which contrasts the behavior in bulk silicon. This fact still leads to number of discussions in the literature and definitely requires further investigation. By determining the intrinsic transconductance values with data obtained from two and four-probe transport measurements, it was concluded that this behavior was due to dopant concentration dependent contact resistances between the Si nanowires and source/drain

electrodes. In other words the contact resistance is negligible for the measurement of transconductance in heavily doped Si nanowire devices, while it makes a substantial contribution in the lightly doped Si nanowires devices. The intrinsic transconductance value was four times larger for the heavily doped nanowires as compared to the lightly doped Si nanowires (Figure 2). The mobility after correction of the contact resistance effects decreased from 260 to 95 cm^2 /Vs as the phosphorous doping level increased from Si:P = 4000 to Si:P = 500 and is in agreement with the values reported for bulk silicon.

As compared with n-type Si nanowire FETs, p-type Si nanowire FETs have attracted greater interest [8, 11, 24, 30, 31, 41-43]. High- performance p-type Si nanowire FETs have been fabricated using 10-20 nm diameter single-crystal VLS grown Si nanowires and Ti as a source/drain (S/D) contact [8]. It was observed that not only was the hole mobility of Si nanowire FETs an order magnitude larger than that of planar Si devices, but the average transconductance was also approximately 10 times larger. However, value of mobility obtained was an estimated field effect mobility based on a measured transconductance. Significantly, it has been observed that the average sub-threshold slope approaches the theoretical limit. Importantly, it has been observed that both the transconductance and mobility increase by an order of magnitude after surface modification, suggesting that many of the electrical properties of the nanowire-based devices are determined by the large number of surface states. These characteristics suggest that Si nanowires have better device characteristics than state-of-the-art silicon-on insulator (SOI) FETs. Si nanowire-based devices thus have the potential to substantially exceed the performance of conventional devices. Nevertheless we should not exclude the fact that such devices lack

the possibility of large scale processability, integration and reliability in their performance.

In order to explore the possibility of utilizing Si nanowire-based FETs in the area of multifunctional electronics and display applications the characteristics of single-crystal Si nanowire FETs assembled on non-conducting glass and plastic substrates have been studied [32]. It was demonstrated that ohmic contacts to Si nanowires are possible on both glass and plastic substrates using post-synthesis processing performed entirely at room temperature. These Si nanowire FETs assembled on both plastic and glass substrates displayed device performances which exceeded those of state-of-the-art amorphous Si and organic transistors currently used for flexible electronics on plastic substrates. Moreover, the high-performance characteristics of Si nanowire FETs assembled on plastic substrates were relatively unaffected by operation in a bent configuration or by repeated bending. The robust nature of Si nanowire FETs on plastic substrates enhances their potential for high performance flexible devices. These studies on Si nanowire FETs on non-crystalline substrates have opened up a new direction for nanoelectronics.

Nanowire FET device performance is affected by the contact properties to a large degree [44-48]. Studies of thermal annealing effects on the transport characteristics of single B-doped Si nanowire FETs with Ti S/D contacts have revealed that both the transconductance and the mobility increase after annealing [8]. Based on measurements carried out on over 50 devices it was concluded that the above observation can be partially attributed to better metal-Si nanowire contacts. Redwing *et al.* have carried out four-point resistance measurements and gate-dependent conductance on individual B- and P-doped Si nanowires grown on the surface of AAO membranes using TMB and PH_3 as the source of

boron and phosphorus, respectively [35, 49]. The results showed a clear trend of decreasing nanowire resistivity for increasing dopant:Si ratio. For P-doped Si nanowires, it was observed that the resistivity decreased by approximately 3 orders of magnitude as the P:Si ratio was increased from 2×10^{-5} to 2×10^{-3}. A P:Si ratio greater than 2×10^{-5} was required to compensate the unintentional p-type background doping (most probably created by the surface states) of the Si nanowires and transition from p- to n-type conduction. A method for extracting Si nanowire resistivity from measurements carried out on B- and P-doped Si nanowire array formed within the pores of an AAO template has recently been developed [50, 51]. This method utilizes the magnitude of the array resistance as a function of nanowire length in order to extract the resistivity parameter. As expected it was found that the resistivity of a nanowire embedded within the AAO membrane decreases with increasing dopant/source gas ratio. Siginificantly, it was observed that the resistivity of these nanowires compared favorably with resistivity data obtained on individual Si nanowires grown under identical conditions. Nevertheless such a relationship is not clear since the structural properties of the free-standing Si nanowires can differ significantly from those deposited within the confined environment of an AAO template.

Silicides can be potentially used as device contacts, gate electrodes, and local interconnects. Self-aligned-silicide technology which offers a possible way to reduce parasitic resistances has been applied for the fabrication of advanced logic devices. This technology may provide a way for the rapid and successful miniaturization of device dimensions for MOSFETs in pace with Moore's law [52-57]. The current focus of silicide technology is centered on contact resistivity in the S/D regions of a MOSFET. The primary challenge

for metallic-S/D technology is achieving a sufficiently low Schottky barrier height to meet the Roadmap I_{on} specifications. Mohney *et al*. have recently described the fabrication of cobalt silicide contacts to Si nanowires within AAO arrays [39]. Cobalt silicide was formed by the reaction of cobalt deposited within the AAO pores and the growing of Si NWs during the VLS process. The interface between the cobalt silicide and Si was formed along the cross section of the wire. However this method may lead to doping of the Si nanowires with Co atoms.

Due to the superior nature of nickel mono-silicide (NiSi) over $TiSi_2$ and $CoSi_2$, such as the elimination of adverse narrow line effects on sheet resistance, lower contact resistance and lower temperature of formation, NiSi is a better candidate to replace $TiSi_2$ and $CoSi_2$ as the silicide material for contact metallization for sub-100 nm CMOS technology [58, 59]. NiSi techonology was first developed by Morimoto *et al* with the demonstration of a 0.4 µm NiSi silicide-based CMOS structure [57, 59]. NiSi can be formed by rapid thermal annealing of a nickel film sputtered onto Si substrates at relatively low temperatures (400-600 °C). The current drivability of both n- and p- MOSFETs with the NiSi technology is higher than the conventional titanium silicide process due to the lower contact resistance and sheet resistance of polysilicon and single-silicon layers. The metal-gate approach is especially crucial for smaller devices with thinner gate dielectrics in advanced CMOS technologies. NiSi used as a metal gate with dual work functions in state-of-the-art thin-body double-gate FINFET structures has been demonstrated. Such MOSFETs with a metal gate are free from the gate poly-Si depletion problem and thus characterized with an enhanced gate control over the channel [56]. Studies on NiSi sub-100 nm gate length CMOS or MOSFETs

have shown that these devices exhibit excellent electrical characteristics [58, 60].

Lieber *et al* have reported the selective transformation of Si nanowires into NiSi nanowires [61]. These single crystal NiSi nanowire heterostructures have ideal resistivities of about 10 μΩ cm and remarkably high failure-current with atomically sharp metal–semiconductor interfaces. Spatially and electronically well-defined metal–semiconductor FETs fabricated based on these heterostructures exhibited a relatively high hole mobility of 325 cm^2 Vs, but lower than previously reported by the same group for doped Si nanowires. The formation of nikel-silicide source and drain segments along the nanowire have allowed the reduction of the physical gate length in Si nanowire FETs (Figure 3) [62]. Si nanowire FETs fabricated using this approach exhibit on/off ratios of up to 10^7, which are the highest reported for catalytically grown and nominally undoped Si NWs.

A surround gate architecture allows better electrostatic gate control of the conducting channel and offers the potential to drive more current per device area than is possible in a conventional planar architecture[63]. With surround gate architecture, FETs offer greater scalability due to the superior control of short-channel effects and leakage, providing the ideal device architecture for sub-10 nm CMOS. The epitaxial growth of vertical nanowires enables the fabrication of surround-gate FETs. The first generation device of vertically integrated nanowire FETs (VINFETs) based on Si nanowires was reported by both Yang and Schmidt in 2006 [63, 64]. The Si wafers on which the Si nanowires were grown served as the common bottom contact. The vertical Si nanowire cores were used as the active channels. The gate length was defined by etching of the gate material. Ti, Ni

or Ni/Pt was fabricated to form the top gate (Figures 4 and 5). No chemical or mechanical polishing step was involved in the fabrication process. This novel concept represents a platform for the fabrication of high-performance Si nanowire electrical devices. Both undoped [7] and B-doped [64] Si VINFETs were fabricated using this technique. The undoped devices functioned as regular FETs having an inverse sub-threshold slope of 250 mV/ decade for small V_{DS}. Under reverse bias, these devices functioned as impact ionization FETs with a $I_{on/off}$ as high as four orders of magnitude. The minimum value recorded was an order of magnitude below the theoretical room temperature limit. Initial first generation un-optimized B-doped Si VINFETs also exhibited excellent electronic properties. The transconductance and hole mobility of these devices was comparable to reported values for high-performance SOI MOSFETs. The sub-threshold slope was much smaller than typical values obtained for nanowire devices with back-gate or top-gate geometries. The authors claim that a Si nanowire channel as thin as 6.5 nm was fabricated, demonstrating the ability to further scale down the device dimensions. Nevertheless, detailed structural characterization demonstrating the very small dimensions of these device were not presented.

3. Germanium Nanowires

Recently Ge has attracted considerable interest as a channel material for FETs due to its lower resisitivity and higher hole carrier mobility compared to Si. These characteristics suggest that Ge nanowires could be utilized in the fabrication of high performance transistors with nanoscale gate lengths, especially for faster switching and higher frequency devices [65, 66].

3.1 Germanium Nanowire Synthesis

The first Ge nanowire synthesis was reported by Heath and coworkers in 1993 using a solvothermal reaction [67]. Other synthetic methods including laser ablation, supercritical fluid-liquid-solid (SFLS) synthesis [68], vapor transport [69] and supercritical fluid (SCF) deposition [40]. Lieber and co-workers have successfully combined the VLS approach with laser ablation techniques for the synthesis of Ge nanowires [70a]. Although single-crystal Ge nanowires with diameters as small as 3 nm have been synthesized using this method the mean diameter obtained is typically around 80 nm. Recently, in-situ high temperature TEM measurements were employed to observe Au-Ge alloy drops at the tips of VLS grown Ge nanowires. It was observed that the phase diagram of the nanoscale drop deviates significantly from that of the bulk alloy, which may explain various discrepancies between actual growth results and predictions made on the basis of the bulk-phase equilibria [70b]. Korgel *et al* have developed high tempertature (375 °C) supercritical fuild-liquid-solid (SFLS) growth approach to grow Ge nanowires ranging from 5 to 30 nm in diameter utilizing organic-monolayer-protected gold nanocrystals as catalysts [68]. Dai and co-workers have reported a relatively low temperature (275 °C) growth of high-quality single-crystal Ge nanowires via chemical vapour deposition (CVD) under atmospheric pressure [71]. A low-pressure CVD method has also been developed to achieve deterministic one-to-one synthesis of Ge nanowires in near-quantitative yields from gold-seeded particles [72]. Tutuc *et al* have studied the morphology of Ge nanowires grown in the presence of B_2H_6. Undoped Ge nanowires wrapped by a conformal B-doped Ge shell were fabricated by a two- stage growth process. The undoped Ge core served as the transistor's channel while the doped Ge shell acted as the gate. The above example opens

up the possibility of a Ge nanowire-based core/dielectric/gate *in-situ* FET growth if a dielectric growth can be introduced before the growth of doped Ge nanowires [73].

Unfortunately, the Ge nanowires synthesized by techniques discussed above are randomly oriented and if nanowires are to be integrated into useful devices it would be highly advantageous to have an organised and aligned array of nanowires. A Langmuir-Blodgett (LB) technique has been used to obtain LB films of high quality single-crystal Ge nanowires with close packing and excellent alignment [74]. These Ge nanowires were synthesized using a CVD approach. The surface of the Ge nanowires was then functionalized and passivated to enhance the solubility of Ge nanowires in organic solvents. Ge nanowire suspension were then added drop wise to a sub-phase of ethanol/water. Floating Ge nanowires were left on the water surface after the evaporation of the organic solvent. The close-packed Langmuir-Blodgett films were then obtained upon compression. Unfortunately, these nanowire arrays lack full directional alignment with controlled pitch and length. Nevertheless isolated nanowires were used for nanowire FET device fabrication [74]. Another approach to form aligned nanowire assemblies was developed by Chidsey and co-workers who grew vertically oriented Ge nanowires of uniform length and diameter [75]. Homogenously-sized gold catalysts from acidified gold colloid solutions were deposited onto oxide-free silicon substrates, followed by a two-step temperature process to grow predominantly vertically-oriented Ge nanowires. Figure 6a shows the cross-section SEM image of vertically-oriented Ge nanowires on Si(111) substrates. 94 % of nanowires were observed to grow in the vertical direction while 6 % of the nanowires were oriented in other non-vertical directions, which appear at 120° from

each other. All nanowires were of the same length. Moreover, it was possible to remove the gold catalysts from the nanowires with aqueous triiodide and HCl while preventing substantial etching of the nanowires. A two-furnace thermal evaporation system where the nanowire growth temperature and source evaporation temperature are separately controlled was developed by Yu *et al* to synthesize large quantities of single crystalline Ge nanowires using Ge powder as a source [4]. A systematic study of the effect of temperature on the Ge nanowire synthesis showed that a high yield of straight nanowires, with relatively good diameter uniformity , were obtained in the temperature range between 450 and 600 °C. Compared to other methods such as laser ablation, metalorganic CVD, and CVD, the two-furnace thermal evaporation system uses a much simpler reaction setup and non-hazardous materials and gases. It was observed that In-catalyzed Ge nanowires prefer [111] growth direction on SiO_2 substrates while [110] direction on Si (111) substrates at the same growth temperature. It was speculated that the low melting point of In and surface interaction between the molten In and different substrates play a key role in determining the growth direction of the Ge nanowires. Nevertheless, a deeper mechanistic study would be necessary to fully identify the growth conditions leading to such deterministic growth directions. High-density, vertical, free-standing Ge nanowires with smooth surfaces and uniform diameters on doped and undoped Ge substrates were produced using a similar approach (Figure7) [66]. The typical morphology of the Ge nanowires consisted of a hemispherical gold catalyst head on top of a Ge receptacle, followed by the Ge nanowire stem. Ge nanowires synthesized using this method were observed to be coated with a thin Ge oxide layer. This approach offers the possibility of integrating nanowires into electronic devices such as VINFETs by avoiding the laborious positioning of

randomly-oriented nanowires, but requires extensive and sometimes limited processability integration steps. Template encapsulation synthesis too offers a viable method to form high density arrays of ordered, crystalline nanowires.

Within CRANN we have developed SCF deposition methods to form high-density, vertically aligned Ge nanowires with controlled diameters. Our synthetic approach for growing Ge nanowires relies on the selective modification of channelled alumina surfaces with Au-seeds that guide the growth of 1 D nanostructures by the SFLS mechanism. The nanostructures were obtained with tuneable and controllable crystallinity, grain size and domain boundaries, ranging from chains of Au-nanoparticles connected through semiconductor Ge crystallites to Au-seeded Ge single crystalline nanowires (see Figure 8). The conditions that control the type of Ge nanostructures produced were: (i) the distribution and size of the Au-seeds across the alumina surfaces, (ii) the type of SCF deposition, *e.g.* batch *vs* flow-through deposition and (iii) the confining environment of the AAO channels.

The synthesis of vertically-aligned Ge nanowires by combining a low temperature nanowire synthesis with the self-assembly of block co-polymer-templated nanoporous films has been reported by Jagannathan *et al* [76]. A 3 nm Au catalyst film was first deposited using electron beam evaporation onto a silicon wafer having 100 nm of thermal oxide. A mesoporous organosilicate film of ~330 nm in thickness was then self-assembled on top of the Au film. The nanowire growth was performed at a partial pressure of 1.8 Torr of germane using a source gas of 10 % germane diluted in hydrogen. All wires in the pores of the organosilicate film were observed to be polycrystalline and the Au catalyst was

found to be present at the tip of the nanowires. The density of the nanowires was found to increase with an increase in growth temperature resulting in close to 100 % filling of pores at 380 °C. Nevertheless the lack of well defined crystallinity and possible integration problems within such a high density nanowire array may hinder further implementation in future electronic devices.

3.2 Germanium Nanowire Field Effect Transistors

Traditional CMOS manufacturing methods for gate electrode formation are not compatible with Ge-based devices as Ge does not grow a stable oxide which is critical for gate electode formation. However the fabrication of Ge-based devices has been made possible by the use of high-*k* dielectrics films such as hafnium oxide and zirconium oxide [77, 78] which have been used to fabricate Ge nanowire FETs. Significantly this approach improves device performance to a certain degree. Using SiO_2 or ALD deposited high-*k* HfO_2 as gate dielectrics, p-Ge nanowire FETs have been fabricated by Dai *et al* using a low-temperature CVD method for both back- and top-gated structures [77, 78]. The back-gated p-type Ge nanowire FETs showed high I_{on}/I_{off} ($\geq 10^3$) and low resistances (~500 kΩ). The hole carrier mobility was higher than 600cm^2/Vs, which is close to the highest reported value for Ge MOSFETs built on Ge wafers (~700cm^2/Vs). As compared to back-gated Ge nanowire FETs, top-gated structures exhibited lower mobility due to the interface states between the HfO_2 and Ge nanowires. Lieber and co-workers have also fabricated p-type Ge nanowire FET [79] which exhibits high currents and transconductances similar to those reported by Dai *et al.* although the mobility in this case was much smaller because of the

unpassivated surfaces of the Ge nanowires. The above examples suggest that a precise control of the doping procedure and surface passivation may possibly provide a solution towards further improving the performance of Ge nanowire FETs.

To date, the bulk of electrical transport measurements reported in the literature have focused on individual nanowires. However there are very few reports on the electrical properties of ordered arrays of nanowires. Within CRANN we have investigated the electrical properties of vertically aligned Ge nanowires within AAO and MTF templates [40, 80] Conductive atomic force microscopy (C-AFM) was used to measure the electrical transport properties of individual nanowires within the arrays, while macrocontacts were used to measure the mean current-voltage characteristics of groups of nanowires (Figure 9). Contact resistance between the nanowires and metal macrocontacts was minimized by polishing and gradual etching the AAO surface, to expose the nanowires, prior to the deposition of the contacts. The C-AFM and macrocontact measurement methods provided approximately the same electrical resistivity results.

3.3 Surface Chemistry of Germanium Nanowire FETs

As mentioned above [65-67], the electrical properties of Ge nanowire FETs are affected by the nature of the surface of the nanowire and hence it is reasonable to expect that passivation and functionalisation of the surface of Ge nanowires before deposition of the dielectric layer would be key step towards fabricating a high-performance device. Korgel *et al* and Dai *et al* have investigated the influence of surface states on the electron transport through both p-type and n-type Ge nanowire FETs [65, 74, 77, 81, 82]. They observed that

hysteresis behaviours in Ge nanowire FETs are caused by water molecules which are absorbed onto the surface oxides of the nanowires due to the electric dipole of the absorbed species. As compared to p-type Ge nanowire FETs, n-type Ge nanowire FETs were observed to be more susceptible to hysteresis behaviour due to Fermi level pining by interface states between Ge and surface oxides. A number of approaches have been utilised to prevent the oxidation of Ge nanowires. For example passivation via self-assembled crystalline monolayers of long chain alkanethiols (≥ 12 carbons) has been used to protect Ge nanowires against oxidation in ambient air [61].. ALD grown high–*k* HfO_2 films could also be applied as the first layer of surface passivation. Thermal annealing in vacuum is also an efficient way to remove the germanium oxides from Ge surfaces and eliminate or reduce the hysteresis for Ge nanowire FETs.

Photoemission studies of the passivation of Ge nanowires grown by cold-wall CVD has revealed that as grown Ge nanowires are initially free of oxide and appear to be hydrogen passivated [83]. The nanowires were observed to progressively oxidize with time when exposed to air. HCl exposure after nanowire CVD growth appeared to produce a Cl passivation which was observed to be more stable than putative hydrogen passivation achieved by aqueous HF treatment.

4. Ge/Si Core/Shell Nanowire FETs

Coaxial heterostructures of two single-crystalline semiconductor materials have significant technological potential. Heterostructured nanowires can serve as building blocks in directed assembled schemes. The interest in the electronic properties in Ge/Si core/shell nanowires is due to the indirect band gaps of Si and Ge [84]. In Ge/Si core/shell

heterostructures, free holes accumulate in the Ge channel when the Fermi level lies below the valance band edge of the Ge core. With this band structure design, it is possible to get high-performance Ge/Si core/shell heterostructure-based FETs.

In 2002, Lauhon *et al* first published their results on the synthesis of core–multi-shell Si/Ge nanowires by a CVD-based epitaxial shell-growth method [85]. A high-performance coaxially gated FET consisted of a core–multi-shell structure: p-Si/ i-Ge/SiOx/p-Ge was successfully fabricated, where the active channel was the Si-Ge shell. This unoptimized device showed a maximum transconductance of 1.5 μA/V, which was comparable to results reported for carbon-nanotube FETs at that time. The coaxial geometry offers advantages for nano-FETs, such as a capacitance enhancements compared to standard planar gates used in nanowire FETs. The most significant success of this geometry is that some key parameters, such as gate dielectric thickness that control the device electrical properties, can be controlled during the initial synthesis stage. All this requires sub-nanometer control during the synthetic steps which in many cases is difficult to achieve and lacks necessary large scale reliability. Nevertheless conceptually these new core-multi-shell structures open up a new platform to study low-dimensional transport phenomena and show the general potential of radial heterostructure growth for the development of high-performance nanowire-based FETs. (Figure 10)

Top-gated single heterostructured nanowire FETs have been fabricated at cryogenic temperatures employing high-k dielectrics with a top gate geometry [10, 84, 86, 87], with Au as the top gate and HfO_2 as the dielectric film (Figure 11). Devices with gate length of 190

nm have exhibited the best performance achieved to date in nanowire FET devices at room temperature. The on current (I_{on}) and transconductance (g_m) were three to four times greater than state-of-the-art Si p-MOSFETs. The sub-threshold slope (S) was superior to the best value reported for nanowire FETs while the hole mobility was much greater than the Si p-MOSFET, Ge and strained SiGe heterostructure PMOS devices. Furthermore, calculated intrinsic delay as a function of gate length for these nanowire FETs showed a significant speed advantage over Si p-MOSFETs. These results have demonstrated that there is great potential for such nanowire devices. The ability to prepare high-performance nanowire FETs with close to 100 % yield could find use in high-frequency electronics on plastic substrates, nanosensors with greater sensitivity, and even extend the roadmap for high-performance logic.

Using Ge/Si core/shell nanowires as building blocks, 3 D, multifunctional electronics can be developed [88]. Both five-layer top-gated single-nanowire FET and ten-layer top-gated multi-nanowire FET have been fabricated based on the layer–by-layer assembly (Figure 12). These devices have exhibited reproducible high-performance. Uniform characteristics and performance has been achieved in sequential layers.

A relative simple method has been developed to fabricate surround-gate (SG) core-shell Ge nanowire FETs based on individual and parallel arrays [9]. The individual SG nanowire FETs have exhibited more desirable on/off ratios and sub-threshold swings than Ge nanowire FETs with planar gate stacks. SG FETs with various numbers of wires, up to 50 in parallel in each transistor, have been fabricated and the electrical properties of such

devices were consistent with that of individual SG Ge NW FETs (Figure 13). It should be mentioned that major difficulties appear to be in the alignment and integration steps that hinder the demonstration of high performance and density of functional nanowire devices.

5. Mechanical Properties of Nanowires

In the drive to implement semiconducting nanowires into devices, their electronic properties have been extensively studied. Nevertheless, mechanical behaviour has received much less attention particularly due to the difficulty in handling these materials which makes manipulation and especially mechanical measurements a considerable challenge. However, the mechanical properties of semiconductor nanowires are of paramount importance in device processing as these building blocks undergo changes in temperature, induced strain and external stress. These stimuli can generate dislocations inside the wire and hence change its electrical conductivity. The processing of VLSI (very large scale integration) induces compressive and tensile stresses via deposition of different materials which can cause failure mainly due to delamination and electro-migration.

One dimensional systems are expected to have interesting mechanical properties due to their high ratio of surface to bulk atoms and the reduced number of defects per unit length. The *Young's modulus* is defined as the ratio of stress over strain, and the *stress* is defined as the ratio of force applied over the area onto which this force is acting. For homogenous materials, simple elastic theory shows that the Young's modulus, E, reflects the average binding forces between the atoms [89]. Therefore, at reduced dimensions, the modulus should become sensitive to the increased fraction of surface atoms and to possible surface tension effects [90, 91]. Different fracture behaviour, enhanced Young's modulii and

strengths or improved elastic properties are expected from nanowires. Many research groups have performed mechanical measurements on individual nanowires, adopting different approaches; predominantly using either an AFM or home-built system incorporated within a TEM.

In 1997, Wong et al [92]studied the elastic strength and toughness of silicon carbide nanorods and multi-walled carbon nanotubes (MWNT) using an AFM based technique. The nanomaterials were first dispersed on a flat surface, and pinned to it by lithographically patterned arrays of SiO_2 squares. An AFM tip was then used to directly measure the force-displacement (F-d) characteristics at different distances from the pinning points and hence the Young's modulus and the bending strength were determined. In addition, a lower boundary for stored strain energy was calculated and showed to be about 10 times higher in MWNTs than in SiC nanorods. This experiment highlighted the potential applications of MWNTs and carbide rods as reinforcement in ceramics or polymer composites. Later, Poncharal and co-workers [93] reported a method involving electrical excitations of MWNTs at their resonance frequency in-situ in a TEM and simultaneously measured the induced dynamic deflection of the tube. The Young's modulus was calculated from the resonant frequency and the dimensions of the wire and was found to decrease sharply with increasing diameter. This was accounted for by the wavelike distortions occurring on the inner arc of bent nanotubes. This method was also applied to a Kelvin probe based on nanotubes and a nanobalance able to measure in the picogram to femtogram range. Yu *et al* [94] used a nano-stressing stage inside a SEM and recorded the entire experiment on video, enabling real-time characterization of the deformation. In

these experiments, individual MWNTs were picked up and attached onto the opposing tips of AFM cantilever probes, as seen in Figure 14. This experiment mimics quite accurately a classical macroscale tensile load experiment and hence allows the calculation of a wide range of mechanical properties, such as the force at fracture, the Young's modulus and the tensile strength. These were found to range from 270 to 950 GPa and from 11 to 63 GPa, respectively. TEM imaging also revealed different fracture patterns such as wavelike structures, ribbon-like distortions and radial collapses [95]. An AFM-based technique was developed by Song *et al* [96] in 2005 and has the key advantage of being non destructive towards the nanowire. An AFM in contact mode scans the surface which is covered with vertically aligned nanowires. The elastic modulus was determined by simultaneously recording the topography and lateral force when the tip scans across the aligned arrays, as shown in Figure 15. Prior to touching a nanowire, a small lateral force is observed (Figure 15(a)). When the tip comes in contact with the wire, the force increases almost linearly as the nanowire is elastically bent from its equilibrium position (Figure 15(b), (c)). At the largest deflection (Figure 15(d)), the tip crosses the top of the wire and the nanowire is then released (Figure 15(e)). However, since no F-d curves were recorded, the behaviour of the wire during manipulation is unknown; it was assumed to be due to bending forces only. This technique was recently improved by Hoffmann and co-workers [97] by setting up an AFM inside an SEM. The AFM tip was used to bend standing silicon nanowires until fracture. The maximum stress before fracture was then calculated and found to be 12 GPa. A correlation between strength and length was also reported, such that shorter nanowires tend to have greater fracture strength than longer ones. In addition, a simulation of the stress showed that the maximum stress appeared at the pinning point of the wire.

An advancement in this AFM technique was developed by Wu et al [98] who overcame the friction issues caused by the nanowires being deposited on a flat surface (Figure 16). This method is very reproducible and provides a wide range of mechanical properties such as Young's modulus, yield strength, plastic deformation and force at failure. Nanowires, pinned on either side of a trench, are laterally loaded by an AFM tip while the F-d curves are recorded. Thanks to a x-y-z closed loop scanner, the tip can be positioned extremely accurately at the loading point (centre of spanning nanowire) and deep enough into the trench to avoid slipping. By imaging the wire before and after manipulation, one can ensure the wire failed at the load point (and not at the pinning points) and that slippage at the pinning lines does not occur. Therefore, the signal recorded is only due to wire deformation. In this manner, the Young's modulus of silicon and germanium nanowires and the maximum strength of germanium nanowires were determined and a generalized model was established [99, 100] for this double-clamped beam configuration. The latter provides a comprehensive description of F-d curves and enables the mechanical properties to be determined. The key advantage of this model is that it accounts for both bending and stretching of the wire, therefore reflecting both linear and non-linear behaviour.

Table 2 presents the values for the Young's modulus (which depends on the crystal orientation) and the fracture strength for bulk silicon and bulk germanium [101, 102]. Table 3 displays the same constants for silicon and germanium nanowires [97, 99, 103-106]. For all the different techniques, the wire systems exhibit elastic behaviour leading to brittle fracture. To date, quite large nanowires have been characterized (over 20 nm in radius), therefore the

elastic constants are close to the bulk values. However, the smallest wires (20 nm in radius) are remarkably flexible as they can be elastically deformed up to 15 times their radii [100]. This ability to store elastic energy suggests potential applications in the field of sensors and nano electromechanical systems (NEMS).

6. Summary and Perspective

1 D nanostructures exhibit critical device function, and thus can be exploited as device elements in future architectures for nanosystems. Semiconductor nanowires are expected to play an important role as building blocks for novel nanoscale electronics assembled without the need for complex and costly fabrication facilities. Several performance requirements outlined in the ITRS roadmap have been demonstrated (such as nanowire length and maximum saturation current density) or are very close to meeting the specification, such as a diameter of 3 nm (< 5nm demonstrated [107]), doping of 10^{18}-10^{19} cm^{-3} (2 x 10^{18} cm^{-3} demonstrated [108]) and resistivity of 5000 - 40,000 μΩ cm (30,000 μΩcm demonstrated [109]), as shown in Table 4. However, some key challenges remain. Progress has been made towards controlling placement of nanowire devices using various approaches such as block copolymer patterning [109]. However reliable angular placement accuracy, specified as 0.6 deg by the ITRS remains to be demonstrated. Nanowire devices typically utilise metal contacts, which can result in ambipolar conduction [110] While the ITRS calls for a contact resistance of less than 10 % of the nanowire resistance, a key challenge will be to achieve this using conventional implanted or diffused p-n junctions. The ITRS also calls for non Au catalysts for nanowire growth for reasons of CMOS compatibility. Additionally, most of the research so far has mainly focused on the growth,

placement and electrical contacting of nanowires but the mechanical robustness of these structures when they are processed into devices needs to be studied in more detail.

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Table 1. ITRS2007 Long-term Technology Requirements—Double-gate MOSFETs (HP: high performance; LSTP: low standby power; LOP: low operation power) [14].

Year		**2016**	**2017**	**2018**	**2019**	**2020**	**2021**	**2022**
Node(nm)		22	20	18	16	14	13	11
Lg(nm)	HP	9	8	7	6	5.6	5.0	4.5
	LSTP	14	13	12	11	10	9	8
	LOP	11	10	9	8	7	6.5	6
V_{dd}(V)	HP	0.8	0.7	0.7	0.7	0.65	0.65	0.65
	LSTP	0.8	0.8	0.8	0.75	0.75	0.7	0.7
	LOP	0.6	0.5	0.5	0.5	0.5	0.45	0.45
$V_{t, sat}$(mV)	HP	*110*	*109*	*114*	*119*	*123*	*115*	*118*
	LSTP	*366*	*371*	*365*	*374*	*378*	*369*	*376*
	LOP	*202*	*188*	*194*	*190*	*195*	*190*	*201*
I_{off}(DG) (µA/µm)	HP	*0.44*	*0.48*	*0.45*	*0.47*	*0.43*	*0.62*	*0.60*
	LSTP	*2.97E-05*	*2.55E-05*	*3.38E-05*	*2.62E-05*	*2.39E-05*	*3.38E-05*	*2.89E-05*
	LOP	*1.31E-02*	*2.23E-02*	*1.94E-02*	*2.55E-02*	*2.41E-02*	*3.26E-02*	*2.40E-02*
I_{on}(DG) (µA/µm)	HP	*2627*	*2533*	*2804*	*2768*	*2677*	*2799*	*2786*
	LSTP	*738*	*839*	*889*	*895*	*935*	*934*	*946*
	LOP	*916*	*808*	*850*	*900*	*919*	*874*	*876*
E_{OT}(DG) (Å)	HP	*5.5*	*5.5*	*5.5*	*5*	*5*	*5*	*5*
	LSTP	*11*	*10*	*10*	*9*	*9*	*8*	*8*
	LOP	*8*	*7*	*7*	*7*	*7*	*6*	*6*

Table 2. Young's modulus (E) and fracture strength (σ) for bulk Si and Ge

	E(GPa)	**σ (GPa)**
Silicon	135-190 [102]	22 [101]
Germanium	103-150 [102]	14 [101]

Table 3. Young's modulus (E), fracture strength (σ) and bending strength (σ_b) for Si and Ge nanowires acquired by AFM techniques and theoretical calculations.

	Si nanowires			***Ge nanowires***	
	E (GPa)	σ (GPa)	σ_b (GPa)	E (GPa)	σ (GPa)
AFM techniques	210 [106], 158 [99], 186 [105]	12 [97]	0.3-0.85 [106], 17.5 [97]	112 [100]	15 [100]
Calculations only: brittle behavior	147.3 [104] (t) 94.43 [104] (c) 165 [103], 139 [103]	22.7 [103] 13.2 [103]		160 [103] 125 [103]	19 [103] 11.1 [103]

t = tetrahedral nanowire, c = cage-like nanowire

Table 3. From ITRS 2007 Table ERM4 Emerging Research Materials - Demonstrated and Projected Parameters [14].

Parameter		**Requirement**
Diameter (nm)	Goal	3-200
	Demonstrated	< 5 [107]- 200 [108]
Angular placement accuracy	Goal	~10^{-2} radians (0.6 deg)
	Demonstrated	-
Length (μm)	Goal	2
	Demonstrated	Si >20 (12 nm diameter)
Doping [electrically active] (cm^{-3})	Goal	~10^{18} - 10^{19}
	Demonstrated	Si ~2x10^{18} (108)
Resistivity (μΩ cm)	Goal	5000 - 40,000
	Demonstrated	30,000 [108]
Contact resistance	Goal	< 10 % nanowire resistance
	Demonstrated	Ohmic
Maximum current density (A/cm^2)	Goal	Bulk
	Demonstrated	I_{Dsat} = 1.94mA/μm (pFET) [111] I_{Dsat} = 1.44mA/μm (nFET) [111]

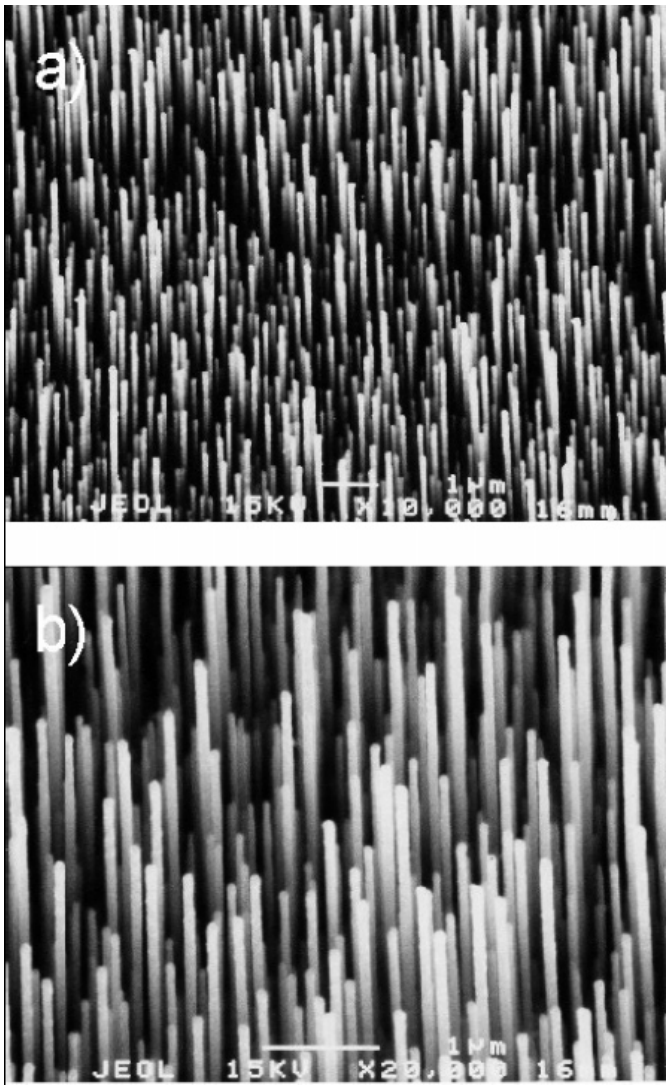

Figure 1. (a) Low magnification and (b) high magnification SEM images of vertically aligned, diameter-controlled Si nanowires grown from ordered Au dots on Si(111) substrates: the average diameter of the wires is 72 nm [36].

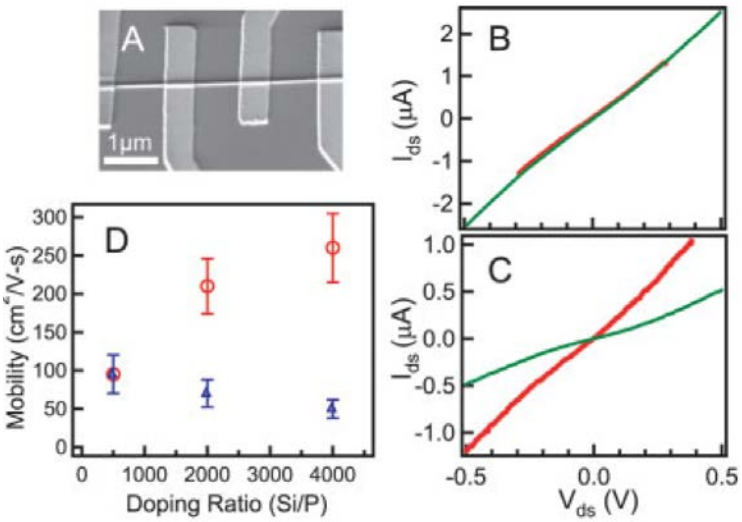

Figure 2. (a) SEM image of a typical Si nanowire device with four contacts used for four-probe transport measurements. (b) I_{ds} versus V_{ds} data recorded on a Si nanowire using two-probe (green) and four-probe (red) contact geometries; the Si/P ratio was 500:1, (c) I_{ds} versus V_{ds} data recorded on a Si nanowire using two-probe (green) and four-probe (red) contact geometries; the Si/P ratio was 4000:1 and (d) measured (blue triangles) and intrinsic (red circles) mobility values, where the intrinsic values were obtained after correcting for contact resistance [41].

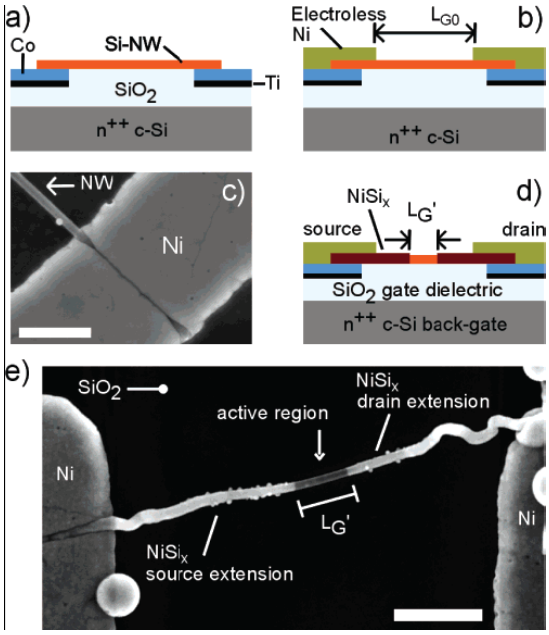

Figure 3. Fabrication of Si nanowire SBFETs with shortened active region: (a) *n*++-Si substrate (common back gate) is covered with a 300 nm thick SiO_2 gate dielectric. Recessed Co/Ti contacts are patterned by photolithography prior to the dispersion of the Si nanowires on top of the substrate, (b) conformal and selective electroless deposition of Ni on Co, embedding the Si nanowires as seen in the SEM top view (c). Annealing leads to Ni silicide segments along the nanowires adjacent to the Ni pads, shortening the length of the active region from *L*G0 to *L*G′ (d) as shown in the SEM top view (e). The scalebars in (c) and (e) are 200 nm [41].

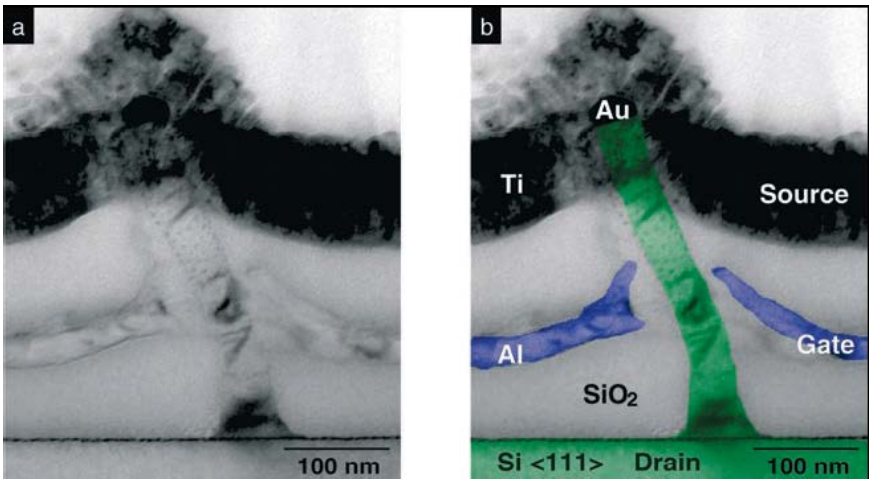

Figure 4. (a) TEM image of a silicon nanowire VS-FET (exclusively produced for TEM study) and (b) colored TEM image (green: silicon, blue: aluminum) [63].

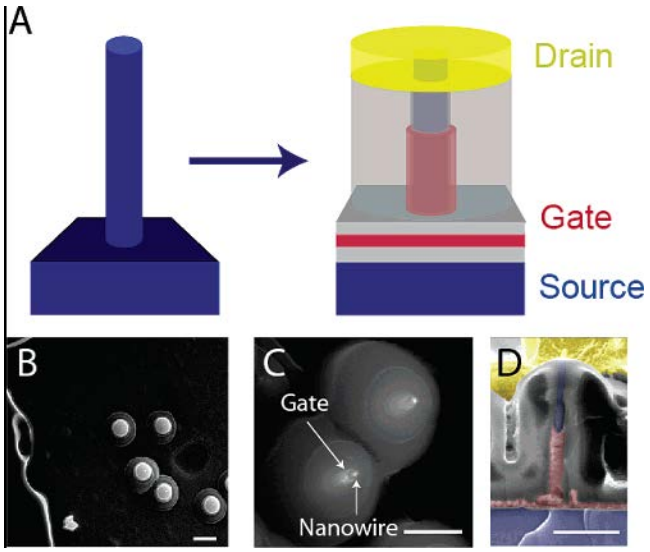

Figure 5. VINFET device configuration: (a) cartoon schematic of a VINFET device (right) fabricated from vertical silicon nanowires (left), (b) top-view SEM image of a completed VINFET device, scale bar is 2 μm, (c) top-view SEM image of the midsection of the VINFET device, highlighting the conformal gate surrounding the nanowire channel, scale bar is 1μm. SEM images (b) and (c) are obtained with a 30^{o} tilt. (d) cross-sectional SEM image of a VINFET device. Scale bar is 500 nm. False color is added to image (d), for clarity. In (a) and (d), blue corresponds to the Si source and the nanowire, gray corresponds to the SiO_2 dielectric, red corresponds to the gate material and yellow corresponds to the drain metal [64].

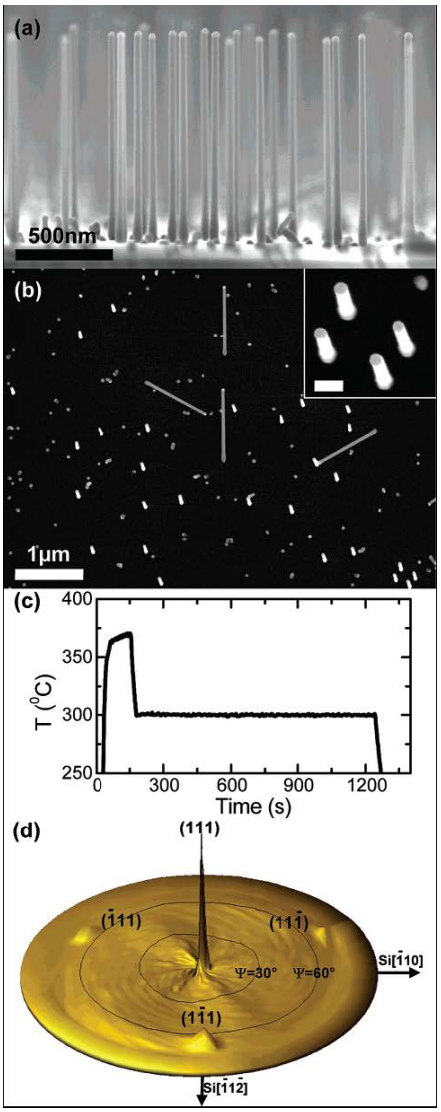

Figure 6. (a) Cross-section SEM of Ge nanowires grown epitaxially on Si(111) substrates from 40 nm gold colloids deposited using the HF-addition method, showing predominantly vertically oriented Ge nanowires of uniform diameter and length, (b) plan-view SEM of the sample in (a) showing the other three ⟨111⟩ growth directions and (b) inset magnified view of vertical Ge nanowires (scale bar is 100 nm), (c) two-step temperature profile used to grow the Ge nanowires in (a) and (b). (d) XRD pole figure of Ge{111} diffraction from the sample shown in (a) and (b) [75].

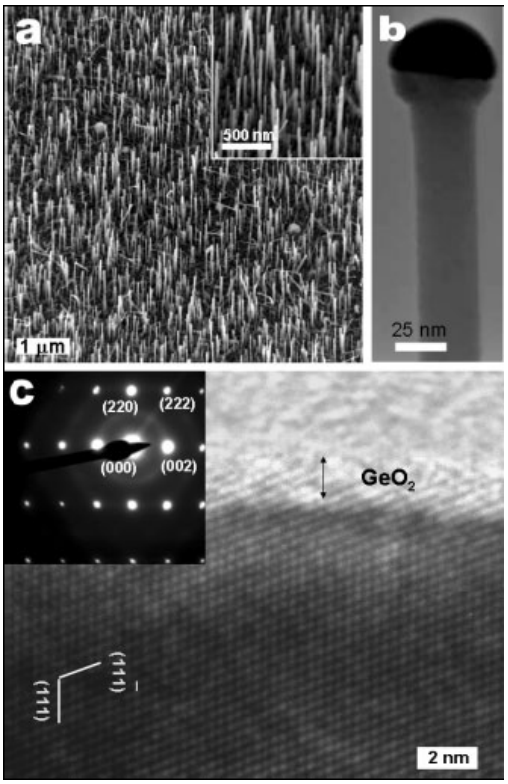

Figure 7. FEG-SEM and high-resolution TEM images of vertical Ge nanowires on Ge substrates: (a) A 30^{o} perspective of high-density vertical Ge nanowires on a (111) Ge substrate. The inset shows a higher magnification of the nanowires, (b) typical nanowires as viewed by TEM, showing a hemispherical alloy catalyst head, a Ge receptacle, and a Ge body with uniform diameter and a smooth surface and (c) a TEM image of the nanowires, showing the (111) lattice friges with an interplanar distance of 3.26 Å, a smooth and distinct boundary between the Ge and the GeO_2 and a GeO_2 sheath of 1-2 nm. The inset shows the electron diffraction pattern suggesting high crystallinity. The spots are resolved to the (300) and (330) families [66].

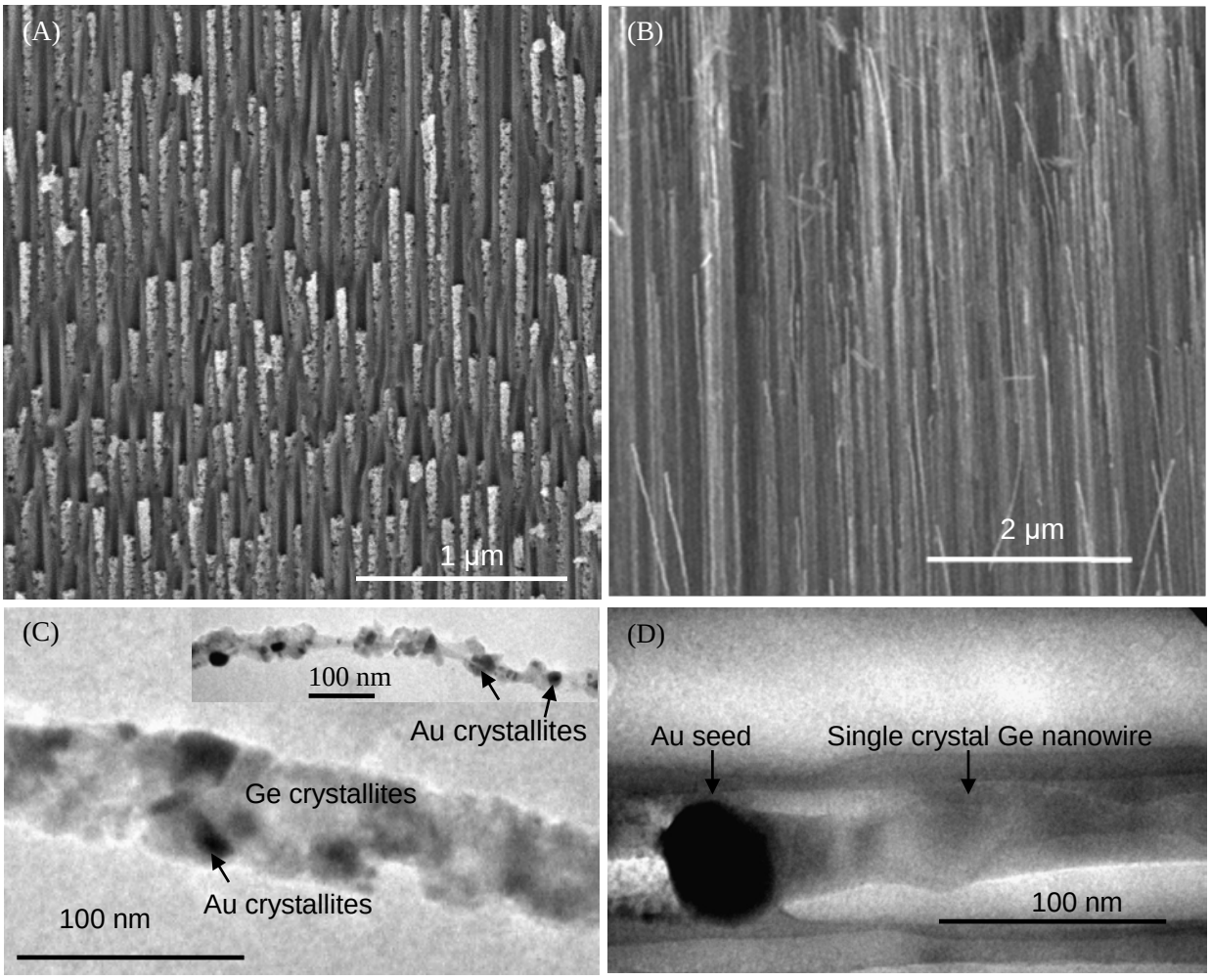

Figure 8. SEM images of (a) polycrystalline and (b) single crystalline arrays of Ge nanowires grown within 80 nm AAO membranes, and (c) and (d) the corresponding TEM images.

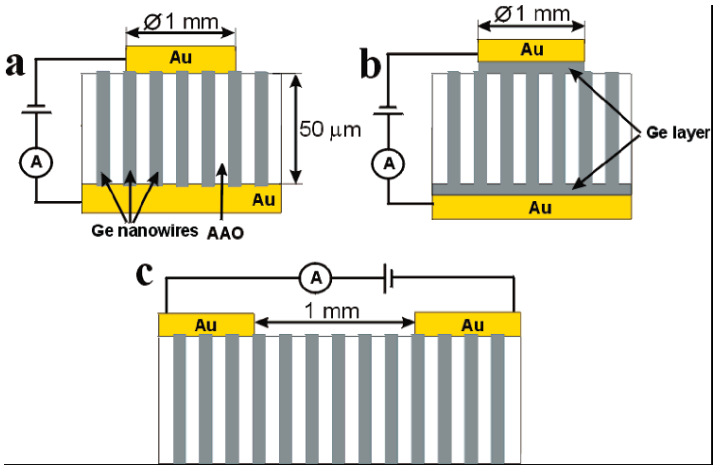

Figure 9. Representation of the macrocontact setup: (a) averaged conductivity through nanowires with Au-Ge nanowire contact interface, (b) same as (a) but with a Ge-Ge nanowire interface and (c) surface conductivity measurement [40].

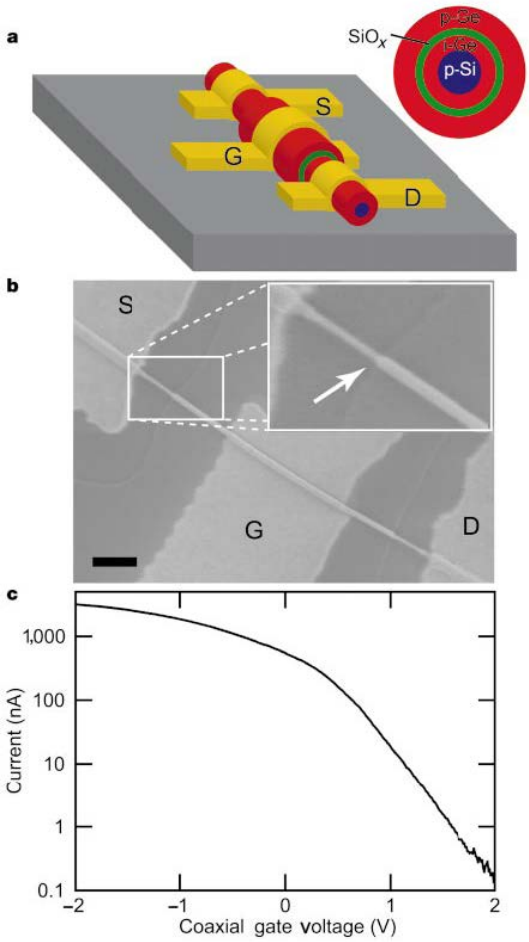

Figure 10. Coaxially-gated nanowire transistors: (a) device schematic showing transistor structure. The inset shows the cross-section of the as-grown nanowire, starting with a pdoped Si core (blue, 10 nm) with subsequent layers of i-Ge (red, 10 nm), SiO_x (green, 4 nm), and p-Ge (5 nm). The source (S) and drain (D) electrodes are contacted to the inner i-Ge core, while the gate electrode (G) is in contact with the outer p-Ge shell and electrically isolated from the core by the SiO_x layer. (b) SEM image of a coaxial transistor. Source and drain electrodes were deposited after etching the Ge (30 % H_2O_2, 20 s) and SiO_x layers (buffered HF, 10 s) to expose the core layers. The etching of these outer layers is shown clearly in the inset and is indicated by the arrow. The gate electrodes were defined in a second step without any etching before contact deposition. Scale bar is 500 nm. (c) Gate response of the coaxial transistor at V SD =1 V, showing a maximum transconductance of 1.500 nA V^{-1}. Charge transfer from the p-Si core to the i-Ge shell produces a highly conductive and gateable channel.

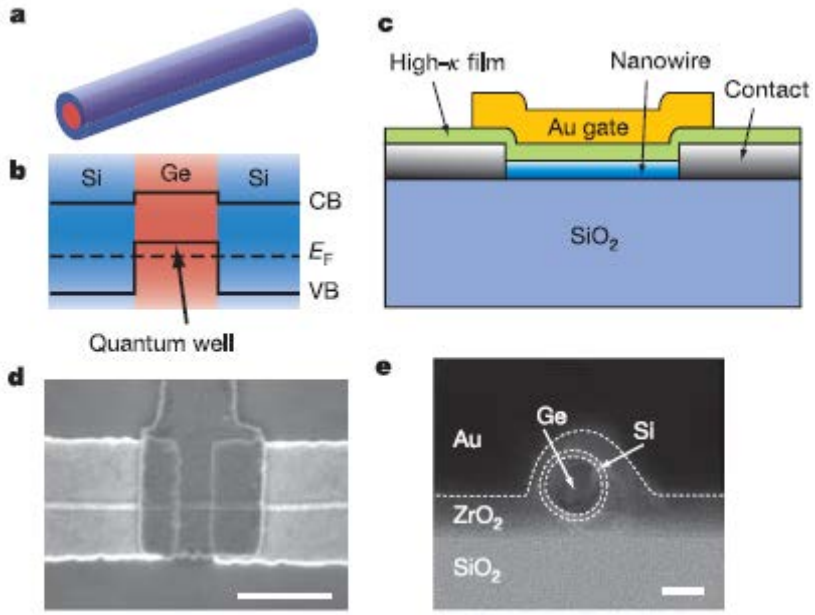

Figure 11 Ge/Si core/shell NWFET: (a) Schematic of a Ge/Si core/shell nanowire, (b) cross-sectional diagram showing the formation of hole-gas in the Ge quantum well confined by the epitaxial Si shell, where CB is the conduction band and VB is the valence band. The dashed line indicates the Fermi level, EF. The valence band offset of ~500 meV between Ge and Si serves as a confinement potential to the hole-gas. (c) Schematic of the NWFET device with high-k dielectric layer and Au top gate. The nanowire sits on a 50 nm thick layer of SiO_2 on top of an n-type silicon wafer with a resistivity less than 0.005 Ωcm. (d) Top-view SEM image of a typical device. The Au top gate overlaps with the Ni source/drain electrodes to ensure full coverage of the channel. Scale bar, 500 nm. (e) Cross-sectional TEM image of a device prepared using 7 nm ZrO_2 dielectric. Dotted lines are guides to the eye showing boundaries between different materials denoted in the image. The nanowire is tilted off the imaging axis. Scale bar, 10 nm [86].

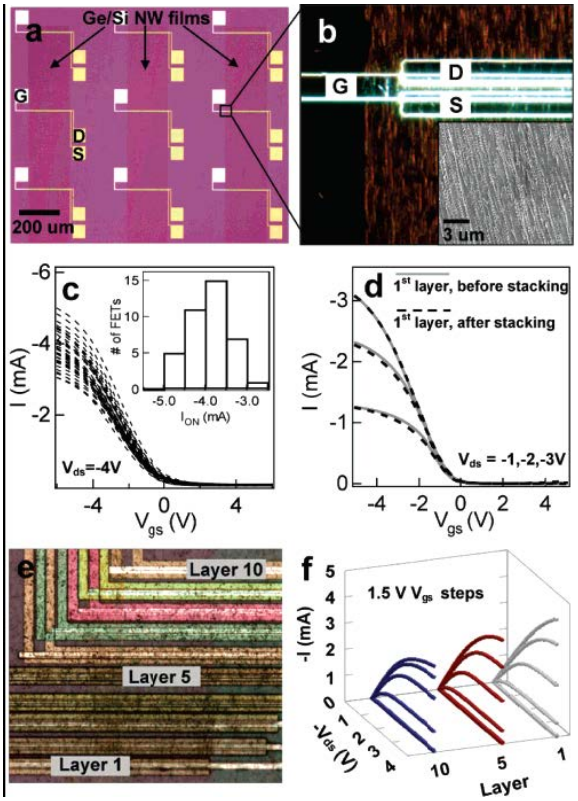

Figure 12. Three-dimensional nanowire FETs. (a) Optical microscope image shows the array of nanowire FETs, (b) dark field image demonstrates a parallel array of nanowires is aligned between source (S), drain (D) and top gate (G) electrodes, (c) *I-V*gs characteristics of 40 NW FETs, (d) transfer characteristics of the first layer NW FET before and after second layer fabrication, (e) optical microscope image of 10 layers of Ge/Si NW FETs. Each device is offset in *x* and *y* to facilitate imaging. (f) Current vs drain-source voltage characteristics (with 1.5 V gate step) for NW FETs from layers 1, 5, and 10 [88].

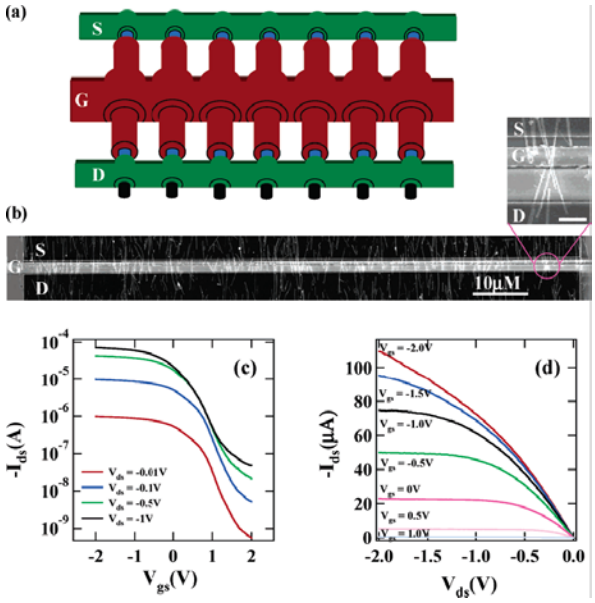

Figure 13. Transistor comprised of multiple surround-gate nanowires in parallel. (a) An idealized schematic presentation of a device, (b) SEM image of a device with ~35 SG nanowires in parallel. Crossing wires (each with its own gate shell) are seen in the zoomed-in image (scale bar = 1 μm) and (c) and (d) transfer and *I*ds-*V*ds characteristics of the device, respectively [9].

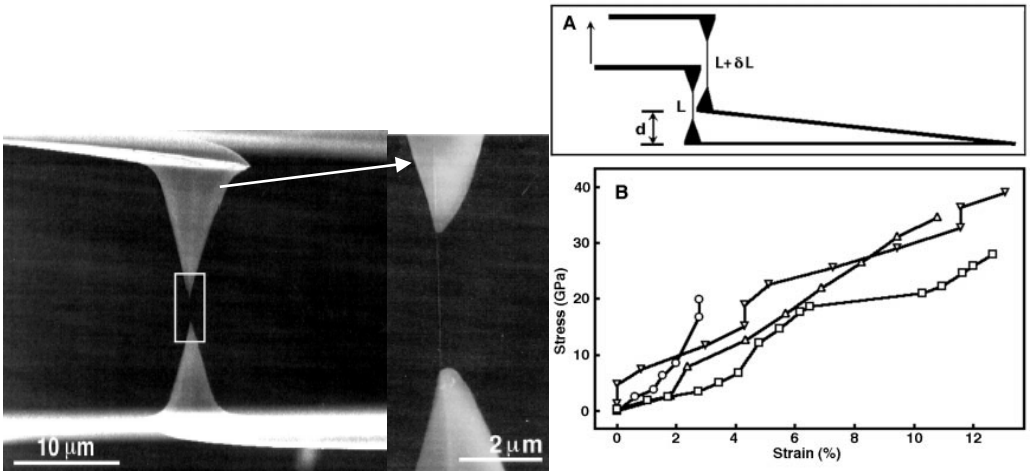

Figure 14. Left hand side: SEM images of the two AFM cantilevers holding a MWNT. Right hand side: (a) schematic showing the principle of the tensile loading experiment. When the top cantilever is driven upwards, the MWNT stretches and brings the lower cantilever with it. (b) Plots of stress versus strain for individual MWCNT [94].

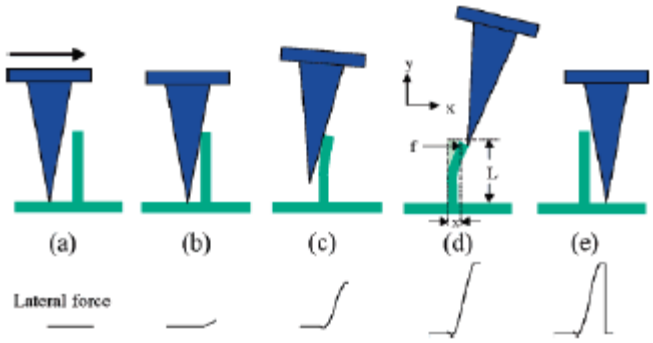

Figure 15. Procedure to measure the elastic properties of an individual nanowire [96].

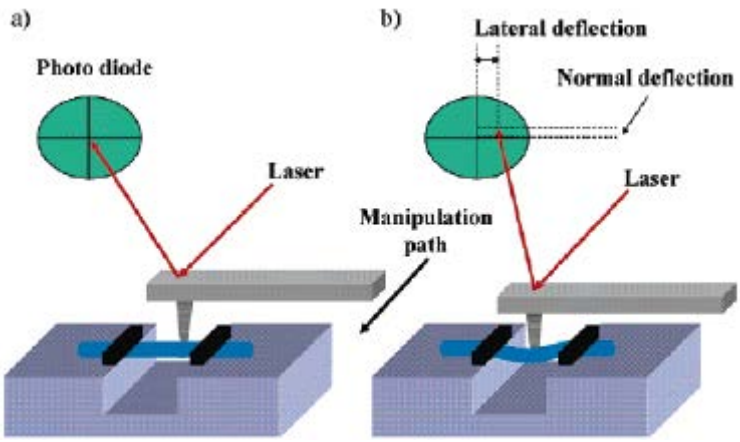

Figure 16. Schematics of the experimental set-up for lateral loading measurements. (a) The tip approaches the pinned wire and (b) during manipulation, the tip pushes laterally on the wire [98].

TOC Graphic & Summary

for *Chemistry of Materials*

Xueyan Wu, Jaideep S. Kulkarni, Gillian Collins, Nikolay Petkov, Dorothée Almécija, John J. Boland, Donats Erts and Justin D. Holmes *Chem. Mater.* **XXXX**, *XX*, XXX One-dimensional Group IV Semiconductor Nanowires: Synthesis, Electrical and Mechanical Properties	In this review, we discuss synthetic methodologies and electrical characteristics of Si and, Ge nanowires and Ge/Si core/shell nanowires. In particular the fabrication and electrical properties of a variety of nanowire-based field effect transistors (FETs) are discussed.