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Study of Interface and Oxide Defects in High-k/$In_{0.53}Ga_{0.47}As$ n-MOSFETs

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***Abstract*— Interface and oxide defects in surface-channel $In_{0.53}Ga_{0.47}As$ *n*-MOSFETs, featuring a threshold voltage, V_T, of 0.43 V, a subthreshold swing, *SS*, of 150 mV/dec., an I_{ON}/I_{OFF} of ~10^4 and a source/drain resistance, R_{SD}, of 103 Ω, have been investigated using "split *C-V*" measurements and self-consistent Poisson-Schrödinger quasi-static *C-V* simulations. An integrated density of traps across the $In_{0.53}Ga_{0.47}As$ band gap at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface, N_{Trap}, of ~ 7.8 × 10^{12} /cm^2, has been obtained from a comparison of the theoretical and experimental quasi-static *C-V* responses, where N_{Trap} reflects the combined contribution of interface traps and border traps. An equivalent surface density of fixed positive oxide charges, N^+, of 1.4 × 10^{12} /cm^2 is also reported. Finally, the application of the Maserjian Y-function to the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS system is briefly discussed.**

***Keywords*— InGaAs; MOSFET; High-k; Split C-V; interface traps; oxide charges; border traps**

I. Introduction

In recent years, $In_xGa_{1-x}As$ *n*-FETs have been the focus of intense research as silicon technology is gradually reaching the limits of dimensional scaling [1]-[4]. $In_xGa_{1-x}As$ offers superior electron mobility but the integration of high-*k* gate oxides still remains a major obstacle to the development of $In_xGa_{1-x}As$ *n*-FETs. In this work, we report on the analysis of interface and oxide defects using surface-channel $In_{0.53}Ga_{0.47}As$ *n*-MOSFETs with Al_2O_3 as a gate dielectric.

The analysis of interface traps in high-*k*/III-V systems is typically based on capacitance and conductance measurements on MOS structures using both *n* and *p* doped semiconductor layers to allow the probing of the upper and lower band gap regions, respectively. The full band gap distribution is subsequently obtained from the combined analysis [5], [6]. The availability of full $In_{0.53}Ga_{0.47}As$ surface channel MOSFETs opens new possibilities as the full quasi static *C-V* (QS *C-V*) response can, in principle, be reconstructed based on the concatenation of the gate-to-channel capacitance, C_{gc}, and gate-to-body capacitance, C_{gb}, measurements. In this work, we explore this approach, where the quasi-static limit is approximated by high frequency (2 MHz) and low temperature (-50°C) measurements of capacitance to minimize the ac response of the interface traps. We compared the obtained C_g-V_g characteristics to the "defect free" theoretical QS C-V response obtained with a self-consistent Poisson-Schrödinger simulator [5], in order to extract the integrated density of traps across the $In_{0.53}Ga_{0.47}As$ band gap at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface, N_{Trap}. As near interface traps (referred to subsequently as border traps) also change occupancy with the slowly varying dc bias on the gate, the approach yields the combined contribution from the interface traps density and border traps density integrated between the $In_{0.53}Ga_{0.47}As$ valance and conduction band edges. Based on the analysis of the experimental and theoretical QS *C-V* responses, the equivalent surface density of fixed positive charges, N^+, present in the Al_2O_3 was also extracted.

II. MOSFET / MOSCAP Fabrication

Surface-channel MOSFETs (Fig. 1) and MOSCAPs were fabricated on a 2-inch wafer supplied by IQE. The wafer structure was a 2-µm-thick Zn-doped (4 × 10^{17} /cm^3) *p*-$In_{0.53}Ga_{0.47}As$ layer grown on a *p*+ InP substrate. The $In_{0.53}Ga_{0.47}As$ surface passivation prior to gate oxide deposition was an immersion in 10% $(NH_4)_2S$ at room temperature for 20 min, which was found to be an optimum in terms of interface trap reduction and for the suppression of native oxide formation [7], [8]. The transfer time to the atomic layer deposition (ALD) reactor after surface passivation was less than 5 min.

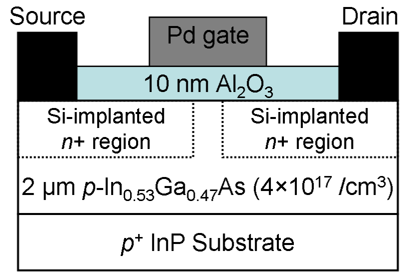


Fig. 1. Schematic cross-sectional diagram of a surface-channel $In_{0.53}Ga_{0.47}As$ MOSFET with a 10-nm thick ALD Al_2O_3 gate dielectric.

A 10-nm-thick Al_2O_3 gate oxide film was formed by ALD using alternating pulses of $Al(CH_3)_3$ (TMA) and H_2O precursors at 250°C. The source and drain (S/D) regions were selectively implanted with a Si dose of 1 × 10^{14} /cm^2 at 80 keV and 1 × 10^{14} /cm^2 at 30 keV. Implant activation was achieved by rapid thermal anneal (RTA) at 600°C for 15 s in a N_2 atmosphere. A 140-nm-thick SiO_2 field oxide was formed by electron beam evaporation and liftoff to minimize the gate pad capacitance. A 200-nm-thick Pd gate was defined by electron beam evaporation and liftoff. Non-self-aligned ohmic contacts were defined by lithography, selective wet etching of the Al_2O_3 in dilute HF and electron beam evaporation of a Au (14 nm)/Ge (14 nm)/Au (14 nm)/Ni (11 nm)/Au (200 nm) metal stack [9]. Finally, a forming gas (5% H_2/95% N_2) anneal treatment was carried out in an open tube furnace at 300°C for 30 min.

III. Results and Discussion

The $In_{0.53}Ga_{0.47}As$ MOSFETs exhibit well behaved transfer and output characteristics, as shown in Fig. 2 (a) and (b), respectively. A threshold voltage, V_T, of 0.43 V, a subthreshold swing, *SS*, of 150 mV/dec., an I_{ON}/I_{OFF} ratio of ~ 10^4 and a source/drain resistance, R_{SD}, of 103 Ω were obtained.

Fig. 3 shows the C_{gc}, C_{gb}, C_g-V_g characteristics, obtained from split *C-V* measurements using an ac signal frequency of 2 MHz and a temperature of -50°C. The C_{gc}, C_{gb}-V_g characteristics were corrected for the overlap and gate pad parasitic capacitances using the method reported in [10]. The C_g-V_g characteristics were obtained from the concatenation of C_{gc}-V_g and C_{gb}-V_g.

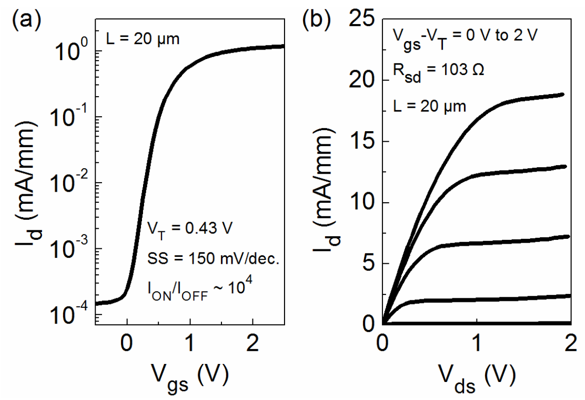
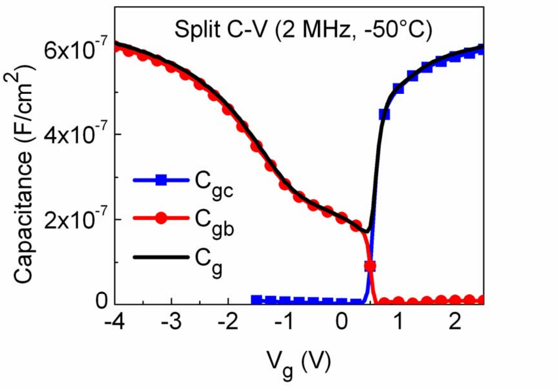


Fig. 2. (a) Log I_d-V_{gs} at V_{ds} = 50 mV and (b) I_d-V_{ds} for V_{gs} ranging from 0 V to 2 V obtained on a 20-μm-gate length and 50-μm-gate width device. The MOSFET features a V_T of 0.43 V, a *SS* of 150 mV/dec., an I_{ON}/I_{OFF} of 10^4 and a R_{SD} of 103 Ω.



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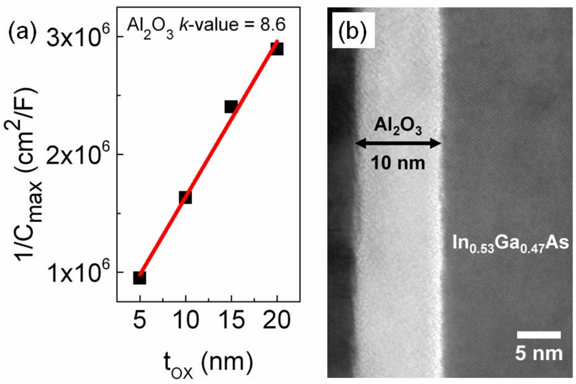

Fig. 4. (a) Inverse of maximum accumulation capacitance, $1/C_{max}$, versus oxide thickness, t_{OX}, for $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs with t_{OX} ranging from 5 nm to 20 nm. (b) Cross sectional HRTEM image through the gate stack region of the MOSFET. A C_{OX} of 7.6 × 10^{-7} F/cm^2 was obtained based on the extracted Al_2O_3 *k*-value of 8.6 and the measured t_{OX} of 10 nm.

The Al_2O_3 dielectric constant, *k*, and the Al_2O_3 film thickness, t_{OX}, were extracted in order to allow accurate QS *C-V* simulation. The Al_2O_3 *k*-value (8.6) was obtained from the slope of the capacitance equivalent thickness in accumulation versus the oxide thickness for $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs with Al_2O_3 thicknesses ranging from 5 nm to 20 nm (Fig. 4 (a)). The cross-sectional high resolution transmission electron microscopy (HRTEM) image through the gate oxide region confirmed a t_{OX} of 10 nm (Fig. 4 (b)). The measured MOSFET gate oxide thickness combined with the extracted Al_2O_3 *k*-value yields a MOSFET oxide capacitance, C_{OX}, of 7.6 × 10^{-7} F/cm^2.

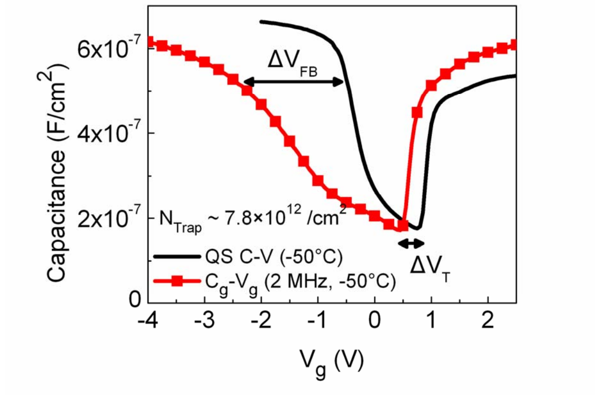

Fig. 5. Comparison of the C_g-V_g characteristics, measured at 2 MHz and at -50°C, to the theoretical QS *C-V* characteristics at -50°C, obtained from a self-consistent Poisson-Schrödinger simulation. An integrated N_{Trap} of 7.8 × 10^{12} /cm^2 and an N^+ of 1.4 × 10^{12} /cm^2 were extracted from this comparison. $\Delta V_{FB} = V_{FB,theo} - V_{FB,meas}$ and $\Delta V_T = V_{T,theo} - V_{T,meas}$.

Fig. 5 compares the reconstructed C_g-V_g characteristics obtained from split *C-V* measurements, using an ac signal frequency of 2 MHz and a temperature of -50°C, with the simulated QS *C-V* at -50°C. In the simulation, the work function of Pd on Al_2O_3, the Al_2O_3 film thickness and *k*-value, and the *p*-$In_{0.53}Ga_{0.47}As$ doping concentration were set to 4.7 eV [11], 10 nm, 8.6 and 4 × 10^{17} /cm^3, respectively. The negative voltage shift of the C_g-V_g characteristics relative to the theoretical QS *C-V* characteristics is attributed to the presence of fixed positive charges in the Al_2O_3 gate oxide film. The stretch of the C_g-V_g characteristics in depletion is due to the presence of interface traps located near the middle of the $In_{0.53}Ga_{0.47}As$ band-gap [12], [7]. The experimental *C-V* stretch out towards the accumulation region could result from a high interface trap density towards the $In_{0.53}Ga_{0.47}As$ valence band edge and/or border traps present in the Al_2O_3 [13]. Measuring the stretch of the C_g-V_g characteristics relative to the theoretical QS *C-V* allows the determination of the overall integrated trap density, irrespective of the nature of the traps, as the additional gate voltage difference between the flat band voltage to the threshold voltage on the experimental C_g-V_g response when compared to the Poisson-Schrödinger QS *C-V* simulation, relates directly to the density of interface traps and border traps integrated across the band gap[1], as expressed in (1):

$$N_{Trap} = C_{OX} \times (\Delta V_{FB} - \Delta V_T) / q \qquad (1),$$

where $\Delta V_{FB} = V_{FB,theo} - V_{FB,meas}$, $\Delta V_T = V_{T,theo} - V_{T,meas}$ and q is the charge of an electron.

[1] For a doping concentration of 4 × 10^{17} /cm^3 in *p*-$In_{0.53}Ga_{0.47}As$, the flat band and threshold voltage conditions related to Fermi level positions are 0.04 eV away from the valence and conduction band edges, respectively. Therefore, selecting the flat band and threshold voltage conditions for 4 × 10^{17} /cm^3 *p*-$In_{0.53}Ga_{0.47}As$ does span the majority of the band gap.

The equivalent density of fixed oxide charges at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface can be determined using (2):

$$N^+ = C_{OX} \times \Delta V_T / q \qquad (2).$$

A theoretical flat band capacitance, $C_{FB,theo}$, of 5.2 × 10^{-7} F/cm^2 and a theoretical flat band voltage, $V_{FB,theo}$, of -0.48 V were obtained from the simulation. A measured flat band voltage, $V_{FB,meas}$, of -2.43 V was obtained, assuming that $C_{FB,theo} = C_{FB,meas}$. The measured threshold voltage, $V_{T,meas}$, of 0.55 V obtained from the split *C-V* measurements differs slightly from that obtained from the *I-V* measurements due to the measurement conditions and *C-V* hysteresis exhibited by the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structure. Indeed, all the *C-V* measurements were obtained using a sweep from inversion to accumulation at -50°C, while the *I-V* measurements were performed the opposite way and at room temperature. Considering a theoretical threshold voltage, $V_{T,theo}$, of 0.85 V and a C_{OX} of 7.6 × 10^{-7} F/cm^2, we calculated a N_{Trap} of ~ 7.8 × 10^{12} /cm^2 and an N^+ of 1.4 × 10^{12} /cm^2 using (1) and (2), respectively. The integrated N_{Trap} value of ~ 7.8 × 10^{12} /cm^2 obtained with this method is consistent with a density of interface traps, D_{IT}, of ~ 5.8 × 10^{12} /cm^2.eV obtained from an analysis of the *SS* (of 150 mV/dec) of the surface-channel $In_{0.53}Ga_{0.47}As$ MOSFET.

The Maserjian Y-function, [14], is of particular interest to the analysis of high-*k*/$In_{0.53}Ga_{0.47}As$ MOS systems. The expression of the Maserjian Y-function is shown in (3):

$$Y = (dC / dV_g) / C^3 \qquad (3),$$

where C is the overall gate capacitance and V_g is the gate voltage. This method allows accurate extraction of V_T, N_a and V_{FB}. Indeed, the Maserjian Y-function peaks at V_T, while its minimum, Y_{min}, is used to obtain N_a and V_{FB} using (4) and (5), respectively:

$$Y_{\min} = -(q \times \varepsilon_{InGaAs} \times N_a)^{-1} \qquad (4),$$

$$Y(V_{FB}) = Y_{\min} / 3 \qquad (5),$$

where ε_{InGaAs} is the $In_{0.53}Ga_{0.47}As$ dielectric constant. Fig. 6 compares the Maserjian Y-functions obtained from the experimental C_g-V_g and the theoretical "defect free" QS *C-V* characteristics. The V_T shift due to the positive oxide charge in the Al_2O_3 is evident (Fig. 6). Y_{min} and (4) yielded a N_a value of 3.3 × 10^{17} /cm^3 (inset Fig. 6), in close agreement with the 4 × 10^{17} /cm^3 specification given to the wafer supplier. The distortion observed on the experimental Maserjian Y-function in the 0 V to -0.5 V voltage region is consistent with a D_{IT} peak located near the middle of the band gap, while the influence of a larger D_{IT} peak near the valence band or a distribution of oxide border traps is visible in the -0.5 V to -2 V voltage region. This distortion in the experimental Maserjian Y-function prevents the extraction of V_{FB}. Further investigations of the mechanisms responsible for the distortion are on-going.

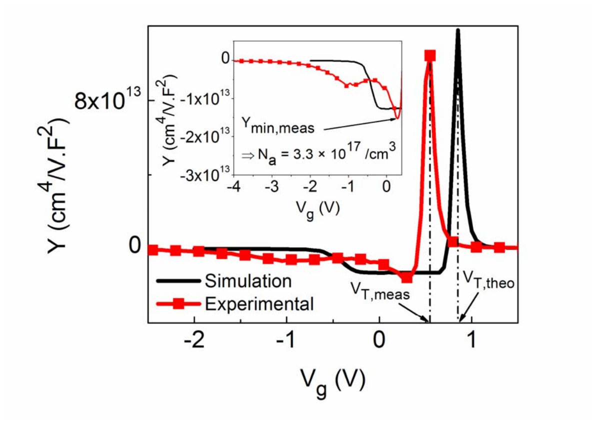

Fig. 6. Maserjian Y-function applied to the experimental C_g-V_g characteristics and the simulated "defect free" QS *C-V* characteristics. Inset: Extraction of a doping concentration, N_a, of 3.3×10^{17} /cm^3 based on the minimum, $Y_{min,meas}$, of the experimental Y-function.

The full paper will include the influence of interface traps on the theoretical Poisson-Schrödinger QS *C-V* simulation and resulting Maserjian Y-function.

IV. Conclusion

We investigated interface and oxide defects in surface-channel $In_{0.53}Ga_{0.47}As$ *n*-MOSFETs using low-temperature high-frequency split C-V measurements and self-consistent Poisson-Schrödinger simulations. An integrated density of traps of ~ 7.8×10^{12} /cm^2 was obtained. This integrated density of traps, including $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface traps and the possible contribution of Al_2O_3 border traps, is consistent with the MOSFET *SS* of 150 mV/dec. An equivalent surface density of fixed positive charges of 1.4×10^{12} /cm^2 was also extracted. Further investigations of the mechanisms responsible for the distortion in both the reconstructed C_g-V_g accumulation characteristics and the Maserjian Y-function are on-going.

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