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Electrodeposited Thin Film Micro-Thermoelectric Coolers with Extreme Heat Flux Handling and Microsecond Time Response

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ABSTRACT Thin film thermoelectric coolers are emerging as a viable option for on chip temperature management of electronic and photonic integrated circuits. In this work we demonstrate record heat flux handling capability of electrodeposited Bi_2Te_3 films of 720($\pm$ 60) Wcm^{-2} at room temperature, achieved by careful control of the contact interfaces to reduce contact resistance. The characteristic parameters of a single leg thin-film devices were measured in-situ, giving a Seebeck coefficient of S = -121($\pm$6) μVK^{-1}, thermal conductivity of κ =

0.85(±0.08) $Wm^{-1}K^{-1}$, electrical conductivity of $\sigma = 5.2(\pm 0.32)\times 10^4$ Sm^{-1}, and electrical contact resistivity $\sim 10^{-11}$ Ωm^2. These thermoelectric parameters lead to a material ZT = 0.26(±0.04), which, for our device structure, allowed a net cooling of $\Delta T_{max} = 4.4(\pm 0.12)$ K. A response time of $\tau = 20$ μs was measured experimentally. This work shows that with correct treatment of contact interfaces, electrodeposited thin film thermoelectrics can compete with more complicated and expensive technologies such as MOCVD multilayers.

Keywords: Thermoelectric Cooler, Electrodeposition, Contact Resistance, CCD – Thermoreflectance, Heat flux.

INTRODUCTION

Thermoelectric materials allow the coupling of electric and heat currents, and can be used to create solid-state heat pumps known as a thermoelectric coolers [1] (TECs). Whilst macroscopic thermoelectric coolers are relatively inefficient compared to other forms of refrigeration, microscale thin film TECs offer a number of advantages. Namely, microscale TECs (μTECs) have a fast response time which scales with their critical dimension, can handle much higher heat flux [2] and they can be fabricated using CMOS compatible processes [3]. Applications of μTECs include thermal management of optoelectronic devices [4], thermal tuning of electronic, photonic and MEMs devices, and sensitive detection of light and heat [5,6]. The problem of hotspot cooling [7, 8] in electronic thermal management is becoming ever more relevant as power densities in electronic circuits rise rapidly. Devices such as processors, light emitting diodes and high frequency GaN HEMTs are producing heat fluxes >500 Wcm^{-2}. Industry has called for innovative cooling technologies to respond to these issues [4]. Integrated microfluidics [9] and two phase cooling [10] have

been proposed as potential solutions, however require a cooling fluid and complicated changes to current layouts and manufacturing processes. The inherent compatibility and simplicity of a solid state thin film thermoelectric devices with conventional CMOS makes μTECs a promising alternative.

Recently, there has been renewed interest in thin film thermoelectric partly due to steady progress in improving thermoelectric material performance. Since the prediction that nanostructuring of thermoelectric materials could substantially improve power factor [11], a plethora of techniques have been investigated which can improve thermoelectric performance. The goal of the materials scientist is to increase the thermoelectric figure of merit (ZT) to maximize performance:

$$ZT = \frac{S^2\sigma}{\kappa}T,$$

where S [μVK^{-1}] is the Seebeck coefficient, σ [Sm^{-1}] is the electrical conductivity, κ [$Wm^{-1}K^{-1}$] is the thermal conductivity of the material and T is the local absolute temperature. The inherent coupling of these parameters makes trying to increase this figure of merit complicated[2]. Recent work has focused on multiscale disorder to reduce the phonon contribution to thermal conductivity while maintaining electrical conductivity [12]. Thin film thermoelectrics allow great control over disorder by using strain, grain boundary control and local doping techniques [13-15]. The advantage of thin film thermoelectrics is that they can handle higher heat fluxes compared to the bulk due to their lower thermal resistance, but a downside is that a lower temperature difference (ΔT) can be sustained across them. Ultimately, to improve micro cooler performance one must optimise both the materials properties and the electrical interfaces with the contacts. In recent years magnetron sputtering [16, 17], pulsed laser deposition [18], and MOCVD [19, 20] have all been used to produce thin film thermoelectrics. Ideally the process must be compatible with the current CMOS fabrication

steps, and as such low temperature synthesis is a requirement. Electrodeposition [21, 22] is a real contender for this, as it is low cost due to its relatively simple process to fabricate materials at low temperatures. The problem with this technique, however, is the inferior electrical properties of the films compared with other solid state deposition techniques, and the relatively high surface roughness. This leads to large bulk and contact electrical resistance of the thermoelectric leg. The maximum heat flux that a TEC can dissipate is limited by self-heating due to electrical resistance. The total resistance can be decreased by making the film thinner, however as contact resistance doesn't scale, the maximum heat flux that can be handled by a thin film TEC is therefore limited by this electrical contact resistance.

In this work we have demonstrated thin film thermoelectric cooling devices with low electrical contact resistance, fabricated from Bi_2Te_3 using a low temperature electrodeposition process. These devices have a reasonable material figure of merit ($ZT=0.26(\pm 0.04)$), and the low electrical interface resistance from our process allows us to make these devices function at a smaller thickness, enabling extreme cooling heat fluxes >700Wcm^{-2}. Low interface electrical resistance σ_c in the range of 10^{-11} - 10^{-12} Ωm^{-2} was measured, which results in an efficient micro-cooler. We attribute this to an Ar-ion cleaning step that removes carbon contamination and activating the surface, and a protective SiN layer which reduces surface oxidisation. We demonstrate that using Tungsten (W) in the top contact material can significantly improve the device operating lifetime particularly at elevated temperatures. We attribute this to the Tungsten acting as an effective diffusion barrier between the Bi_2Te_3 and the Au top contact. Finally, we demonstrate that the microscale thermoelectric pads we developed have an extremely fast time constant ~20 μs, which would enable real time temperature control of electronic and photonic devices, and significantly reduce temperature control energy requirements at chip scale.

RESULTS

A cross section of the device structure examined is shown in Fig. 1a. The Bi_2Te_3 thin film is synthesized using the electroplating technique described in the methods section, and the metal contacts are deposited using electron beam evaporation. The Bi_2Te_3 is isolated from the silicon substrate with an insulating layer of SiO_2 as seen in Fig. 1a. A 300 nm layer of SiN is deposited immediately after the electrodeposition in order to prevent surface oxidation of the film and to allow electrical probing of the top contact without damaging the film surface. In the next step an

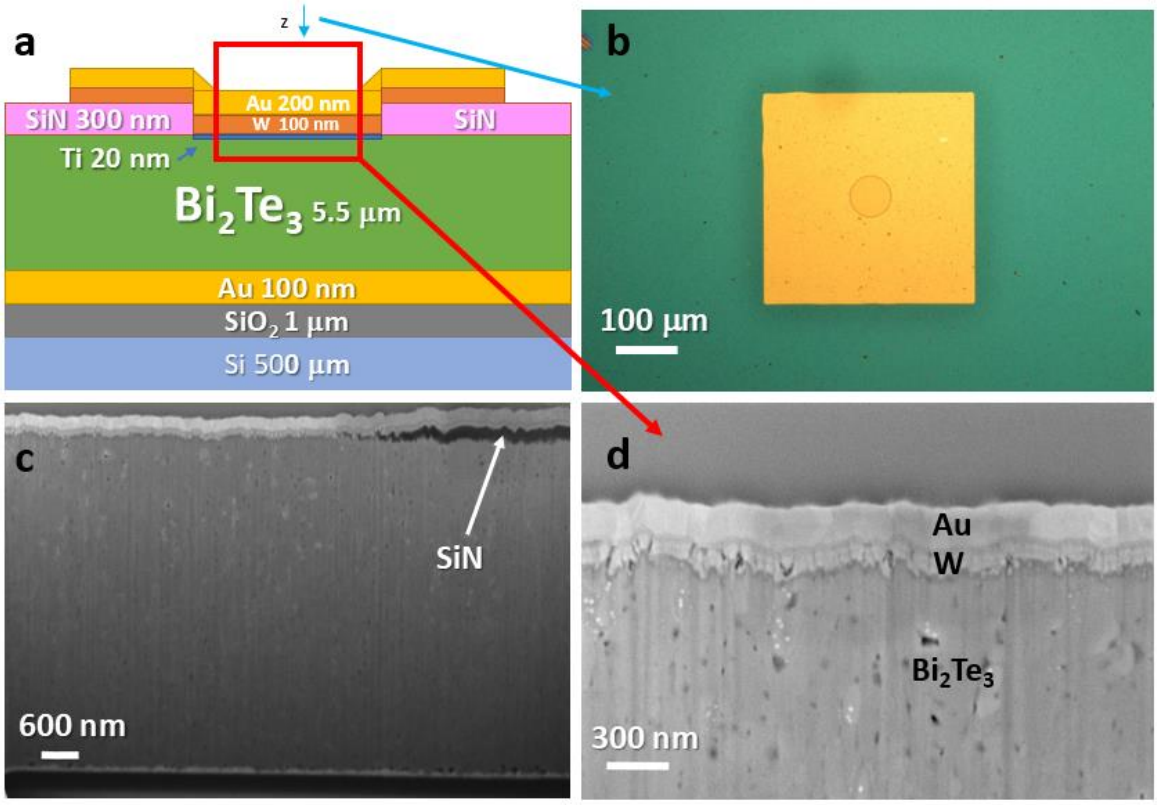


Figure 1 Device structure and cross section. (a) Schematic cross section of a single device structure showing top and bottom contact structures. **(b)** Optical image of the 80 µm diameter pad with 400 µm side. **(c)** FIB cut SEM cross section of the contact region showing SiN layer transition. **(d)** FIB cut SEM image of the interface of the top contact showing both tungsten and gold layers.

in-situ Ar-ion cleaning step is used to prepare the Bi_2Te_3 surface, and then metallic cylindrical top contacts are deposited to a total thickness of 500 nm using electron beam evaporation. The contacts are lithographically defined with diameters ranging from 22 μm to 145 μm. Tungsten is chosen as the initial top contact metal with an aim of inhibiting the diffusion between the TE material and top contact which can increase electrical contact resistance [23] . Finally, larger square contact pads, of side length 400 μm, are deposited using a shadow mask aligned with the electrode array as shown in Fig. 1b. This allows electrical probing of the top contact without obscuring or damaging the active region, and helps to reduce measurement errors due to heat transfer resulting from probe contact resistance and thermal bridging. We found that the ion cleaning step was critical to achieving low electrical contact resistance, whereas the SiN layer was required in order to achieve repeatable measurements using direct electrical probing. Samples with tungsten diffusion barriers showed much better long term stability as compared to those without. (Supplemental Fig. S1) Cross sectional SEM of the electrodeposited samples Fig. 1c and Fig. 1d show that there is a surface roughness with RMS 30 nm on the Bi_2Te_3 layer and ~30% porosity in the films respectively. The edge from the contact to the SiN insulated region is shown to transition gradually over a 1 μm length scale.

Electrical conductivity and interface resistance measurements:

The electrical resistivity of the thin Bi_2Te_3 film and the interface conductivity of the top contact were both measured using the Cox-Strack method. This technique works by creating an array of top contacts with diameter varying on a range similar to the thickness of the film. In our case we made contacts ranging from 22 μm to 145 μm in diameter with the optical images of the smallest and largest contacts shown in Fig. 2a. The dependence of the total device resistance R_t on contact diameter is given by [24]:

$$R_t = \left(\frac{4R_c}{\pi}\right)\frac{1}{d^2} + \frac{\rho}{\pi}\arctan\left(\frac{4}{d/t}\right)\frac{1}{d} + R_0 \qquad (1)$$

Where R_c [Ωm^2] is the top contact resistance, d [m] is the contact diameter, ρ [Ωm] is the resistivity of the Bi_2Te_3 layer, t [m] is the thickness of the layer and R_0 [Ω] is the total back contact resistance. The first term shows that the contribution of top contact interface resistance decreases as the inverse of the area of the contact. The second term accounts for the bulk resistivity including arctan term which accounts for current spreading. R_0 takes into account the contribution of the top gold contact as the distance between the probe and centre of the circular pad was kept consistent throughout the measurement. The maximum resistance of the gold and tungsten circular pad layers

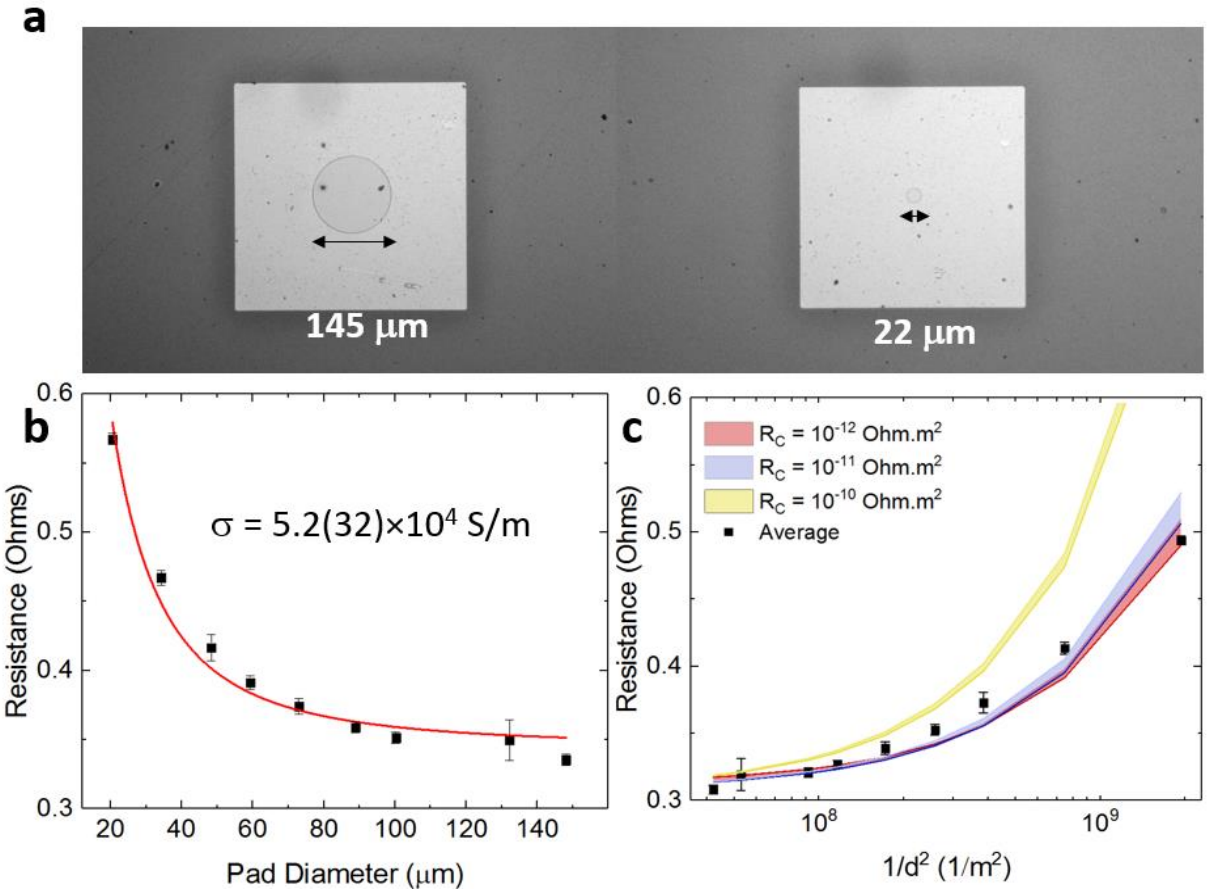


Figure 2. Electrical conductivity and contact Resistance measurements. (a) Optical images of test pads showing contacts with 145 µm and 22µm diameters. (**b)** Measured 4-point resistance as a function of pad diameter, with fitting of equation 1. (**c)** Total resistance vs $1/d^2$ overlaid with analytical model showing effect of contact resistance on total resistance.

126 can be calculated to be 1.5×10^{-5} Ω for the smallest pad diameters. This is a negligible contribution
127 to the total device resistance which is around 0.2 Ω for the smallest pads. Fitting the experimental
128 data with this equation as shown in Fig. 2b allows us to extract that the Bi_2Te_3 conductivity at σ =
129 $5.20(\pm0.32)\times10^{4}$ Sm^{-1} at room temperature. This is roughly 50% of the value of the bulk
130 conductivity, but comparable to other n-type thin film electrodeposited Bi_2Te_3 [25-28]. This reduced
131 electrical conductivity can be attributed both to the low carrier concentration of the Bi_2Te_3 and the
132 non-negligible porosity of the electrodeposited films as shown in Fig. 1d. The porosity will
133 decrease the electrical and thermal conductivities in a similar fashion so does not appreciably
134 degrade the ZT. Plotting the data against $1/d^2$ in Fig. 2c we can clearly see the effect of contact
135 resistance. Fitting this data we can put the contact resistance in the range of $R_c \sim10^{-11}$-10^{-12} Ωm^2.
136 This equates to a contribution of less than 2.6 mΩ (1.3%) of the total device resistance for the
137 smallest pad which shows that the contact resistance has a negligible effect in this case. The effect
138 of a typical contact resistance of 10^{-10} Ωm^2 raises the value of total resistance outside of our
139 experimental data as shown in yellow in Fig. 2c. Our measured contact resistance is at the lower
140 end of previously reported contact resistance measurements for magnetron spluttered [29] and
141 chemical vapour deposited [30] Bi_2Te_3 thin films, which were on the order of 10^{-10}-10^{-11} Ωm^2 . This
142 low interface resistance is key to achieve high heat flux handling capability. 3D FEM simulations
143 show that net cooling can only been seen in this device if the contact resistance is less than 10^{-11}
144 Ωm^2 (Supplemental Fig. S2.)

145 Thermal property measurements: The thermal conductivity, volumetric heat capacity and
146 thermal interface resistance of the thin Bi_2Te_3 films were measured using a custom-built frequency
147 domain thermoreflectance (FDTR) setup described in the methods. Briefly, FDTR uses a
148 modulated pump laser to provide a periodic heat source, which results in an oscillation of the

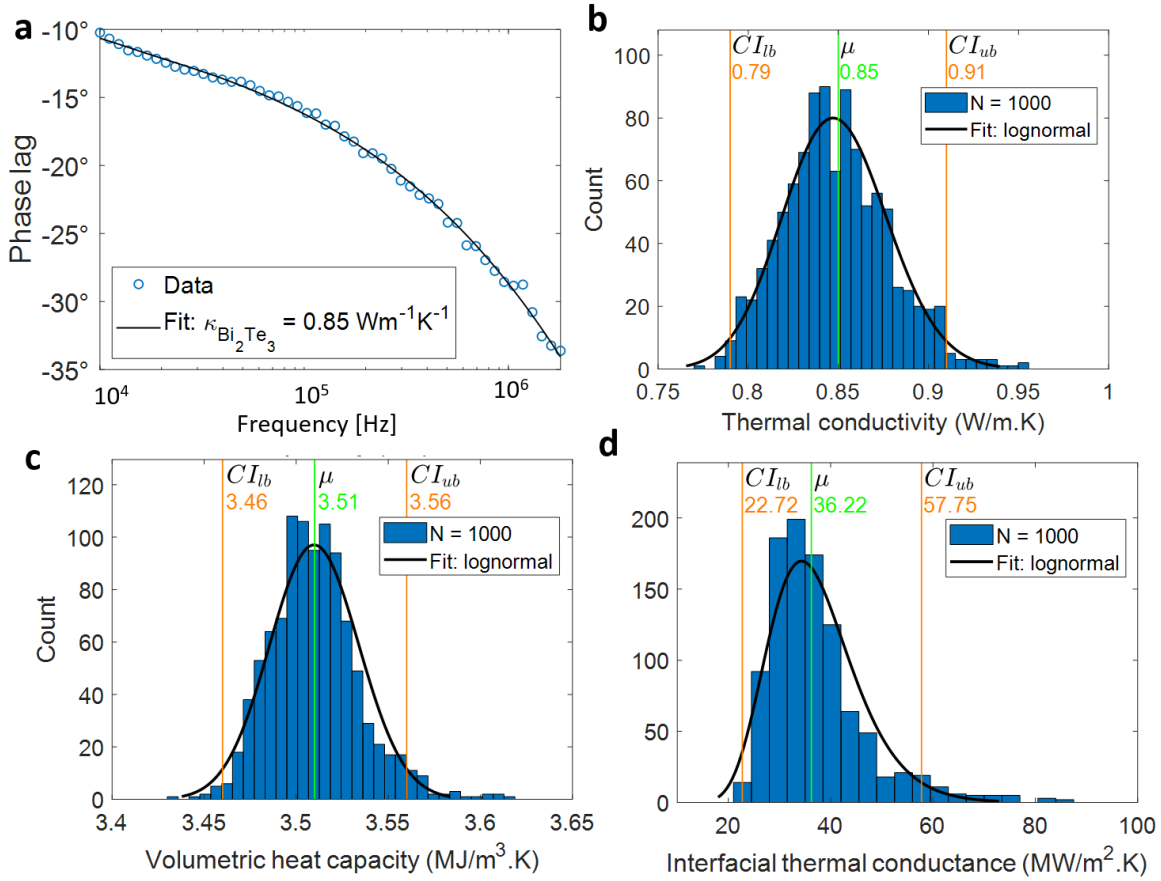


Figure 3. Measurement of Thermal properties. **(a)** Measurement of the temperature oscillation phase lag in degrees from the pump laser from FDTR technique. **(b)** Extracted thermal conductivity that fits from 1000 fittings using Monte Carlo method, κ=0.85±0.08 Wm^{-1}k^{-1}**(c)** Fitted volumetric heat capacity C=3.51± 0.05 MJm^{-3}K^{-1} **(d)** Fitted Interfacial thermal conductance between Bi_2Te_3 and Au G=36±21 MWm^{-2}K^{-1}

surface temperature. The surface temperature can be measured using a separate probe laser through the temperature dependent change in the surface reflectivity. The frequency of the modulation is scanned from 100 Hz to 50 MHz. The phase lag of the temperature oscillation are measured and can be fitted with a transfer matrix model to extract the thermal properties of a layered thin film structure [31] as shown in Fig. 3a. Tuning the frequency effectively tunes the thermal penetration depth allowing separation of thermal conductivities and interface conductance's in multi-layered structures. This technique is particularly useful as compared to more standard techniques such as time domain thermoreflectance (TDTR) as there are no moving

parts such as a delay line which introduce additional uncertainty. The local nature of this measurement allows us to measure the thermal properties on a single device pad. Using this technique we extract a value for the thermal conductivity of the electrodeposited Bi_2Te_3 film of 0.85($\pm$0.08) $Wm^{-1}k^{-1}$ (Fig. 3b), volumetric heat capacity of C=3.51$\pm$ 0.05 $MJm^{-3}K^{-1}$ (Fig. 3c), and interfacial thermal conductance between Bi_2Te_3 and Au of G=36$\pm$21 $MWm^{-2}K^{-1}$ (Fig. 3d). The thermal conductivity is the critical parameter for device performance and is in line with measured values in similar films in the literature which range from 0.7–1.48 $Wm^{-1}K^{-1}$ [32-35]. The uncertainty in this measurement is the largest of the characterisation steps used. As such in the resulting simulations the extreme edges of this conductivity range will be shown to show the uncertainty in the simulations. The thermal conductance is relatively high between the Bi_2Te_3 and contact and contributed a negligible 0.47% to the total thermal resistance of a typical 22 μm diameter device.

Seebeck Coefficient measurements:

An accurate measurement of the Seebeck coefficient is necessary to calculate ZT and predict the device performance. This requires precise control of the top and bottom contact temperatures while measuring the open circuit voltage across the device. Due to the thin film nature of the device, knowing the true temperature drop across it can be difficult and lead to large measurement errors. In this case, we decided to use a novel technique to measure the Seebeck coefficient by using a CW (continuous wave) laser to provide a uniform heat flux into the top surface of the device. We then measured the local temperature rise of the top contact using thermoreflectance imaging while simultaneously measuring the open circuit voltage. An aperture is placed conjugate to the image plane of the microscope objective creating a top-hat intensity profile to create a uniform heat source. An optical image of a 22 μm diameter pad is shown in Fig. 4a with a temperature map of the surface taken using CCD based thermoreflectance (CCD-TR) shown in Fig. 4b. CCD-TR is a

lock in thermography technique which allows sub micro resolution temperature mapping as described in methods. We cannot directly measure the temperature at the bottom contact and must infer this from 3D FEM simulations using the thermal conductivity measured previously from the FDTR results. The error in this measurement is therefore related to how well we know the thermal conductivity of the device. This is seen in Fig. 4c and Fig. 4d where the red and green lines signify the extremity of the possible thermal conductivities, between 0.77 and 0.93 $Wm^{-1}K^{-1}$ respectively. In Fig 4c we first use CCD-TR to map the surface temperature as a function of incident irradiance.

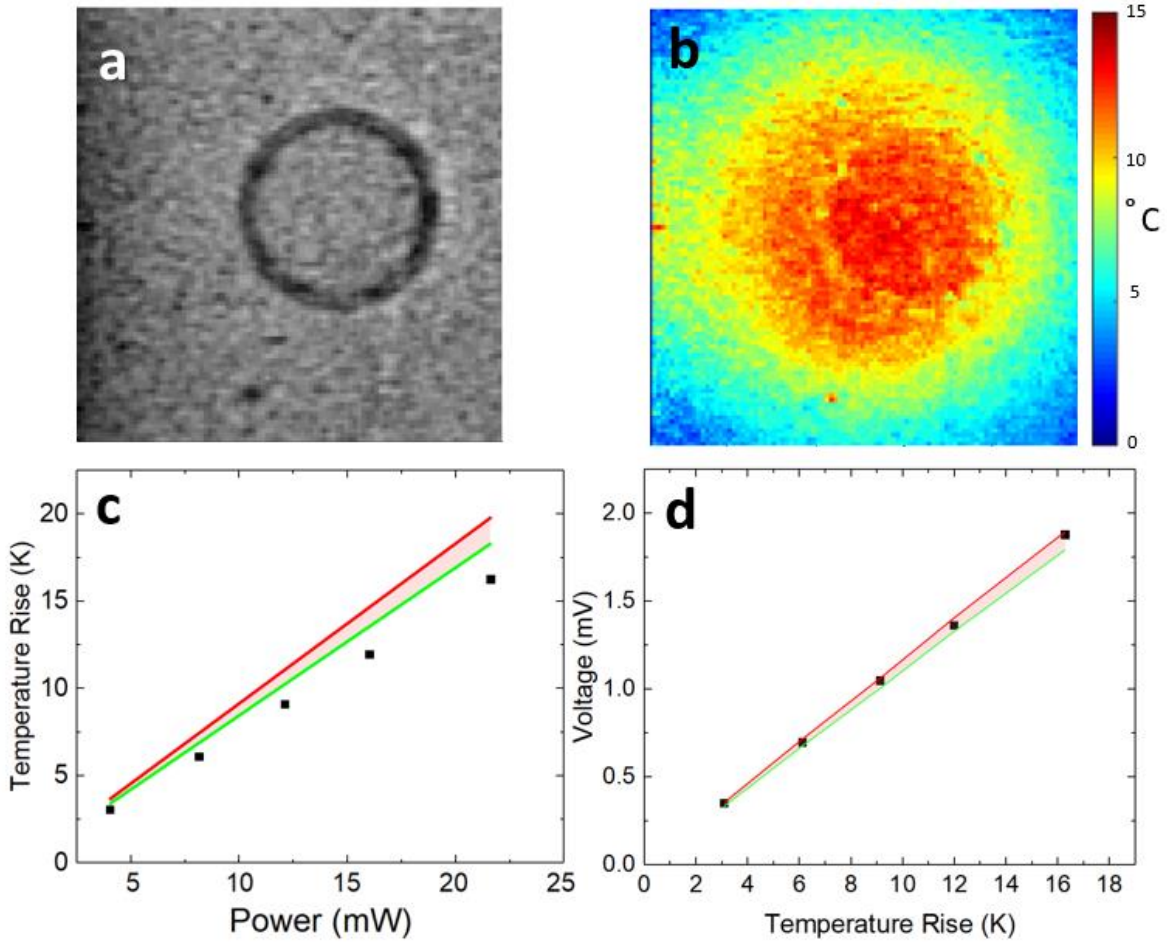


Figure 4. Seebeck coefficient measurement. (**a)** Optical image of 22 μm diameter pad. (**b)** Temperature map by CCD-TR resulting from 20 mW 488 nm laser incident on same pad. (**c)** Average top contact surface temperature measured using CCD-TR vs incident laser power. **(d)** Voltage produced from temperature differential as a function of top contact temperature Red/Green lines denote simulated results for extremes of thermal conductivity error from 0.77-0.93 $Wm^{-1}k^{-1}$ respectively.

Discrepancies between the model and experimental results in Figure 4c are attributed to the use of a constant property model as described in the modelling method section. From this temperature rise, we can measure the open circuit voltage and plot this against top contact temperature as shown in Fig. 4d. Using the slope of this graph would underestimate the Seebeck coefficient as we would be assuming that the bottom contact temperature remains at room temperature under laser illumination. From our FEM simulations we know this is not the case, one must extract the bottom contact temperature and calculate the true temperature difference across the device to accurately calculate Seebeck coefficient. Instead we modelled various Seebeck coefficients to find the best fit for the voltages produced. Using this technique, a Seebeck coefficient of S= -121 ($\pm$6) μVK^{-1} was consistently measured on a range of different contact pads. This value is consistent with previous n-type Bi_2Te_3 materials reported in the literature [36-38].

Device performance under zero heat load:

The performance of the device under zero heat load can be determined by measuring the surface temperature for a range of input currents. Figure 5a shows a typical temperature map recorded with the CCD-TR technique at 100 mA current applied such as to heat the top surface. As the material is n-type, this is achieved with a negative current terminal at the top surface. The polarity can be reversed to cool the top surface. Fig. 5b shows a cross sectional temperature map of the device in cooling mode. It shows that as heat is pumped from the surface to the substrate there is a reduction in temperature at the surface and a corresponding increase in temperature at the bottom contact.

These FEM simulations can be used to predict the surface temperatures for particular input current and compare with the experimentally measured data. These compare well considering the 10% error in thermal conductivity measurement as shown in Fig. 4c. The slight discrepancy in the

heating mode is attributed to the temperature dependence of the Seebeck coefficient, thermal and electrical conductivities which were not taken into account. We see a net cooling of up to 4 K in our devices which confirms our measured low contact resistance. We attribute this low interface resistance to the low surface roughness of 20-30nm and ion cleaning steps used in device fabrication. This in-situ technique ensures removal of any oxide layer or adsorbed water molecules before deposition of the top contact.

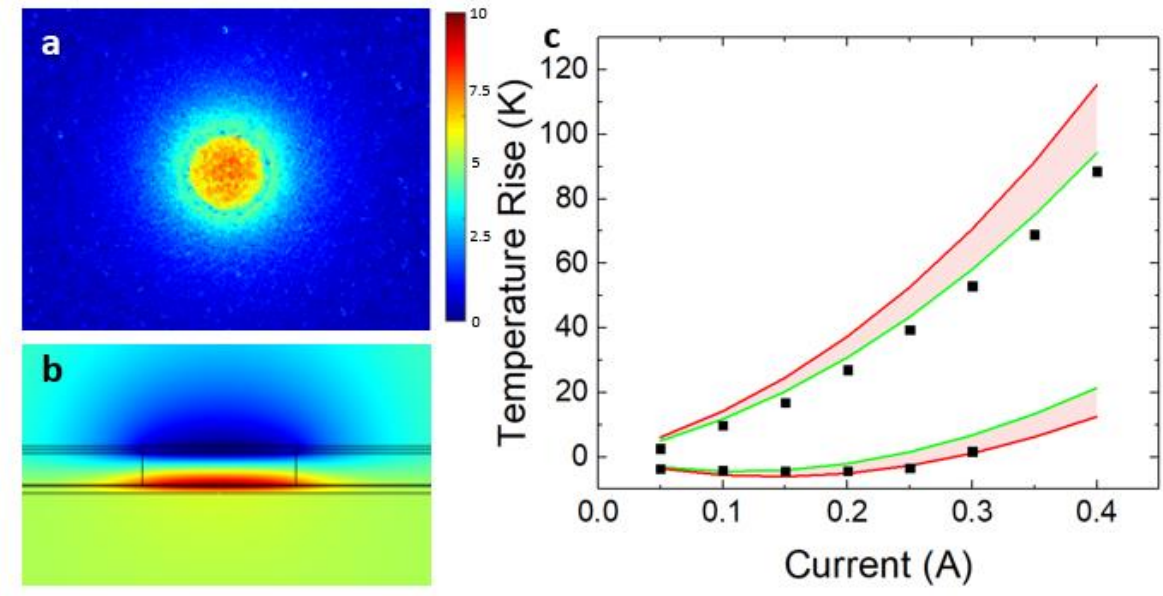


Figure 5. Device performance under zero heat load (a) Temperature map showing cooling for a 100 mA applied heating current. **(b)** Simulation showing the temperature distribution for a cross section of the device. **(c)** Mean temperatures of pad for various heating and cooling currents, red/green lines denoted simulation results over the error range of the thermal conductivity measurement. 0.77-0.93 $Wm^{-1}K^{-1}$.

Device time response:

Fast time response for cooling and heating are important for temperature control in optoelectronic applications such as laser and diode temperature tuning. In this work we show that the time response of these devices is on the order of 20 μs or less for the 22 μm diameter contacted devices. This is up to two orders of magnitude faster than the current state of the art devices [39, 40] and a million times faster than a standard macro scale commercial Peltier cooler. This is to be

expected from the small cross-sectional area of the active thermoelectric material. Temperature profiles are extracted from time dependent FEM simulations and shown at 5 μs time steps for heating (Fig. 6a) and cooling (Fig. 6b) regimes. Fig. 6c shows that heating using a microscale thermoelectric device can be significantly faster than resistive heating alone. The mean heating and cooling rates are extracted as 0.34 $K\mu s^{-1}$ and 0.44 $K\mu s^{-1}$ respectively. These are over 5 times faster than if the device was purely resistive in nature, with a resistive heat rate of 0.06 M $K\mu s^{-1}$. The response time was measured directly by locking into the changing thermoreflectance signal as a 50% duty cycle square current source is applied. Whilst the signal was quite noisy, one can see that the simulated FEM results fit quite well when overlaid onto the data in Fig. 6d. The thermal response times can be changed by increasing/decreasing the pad diameter. The time constant

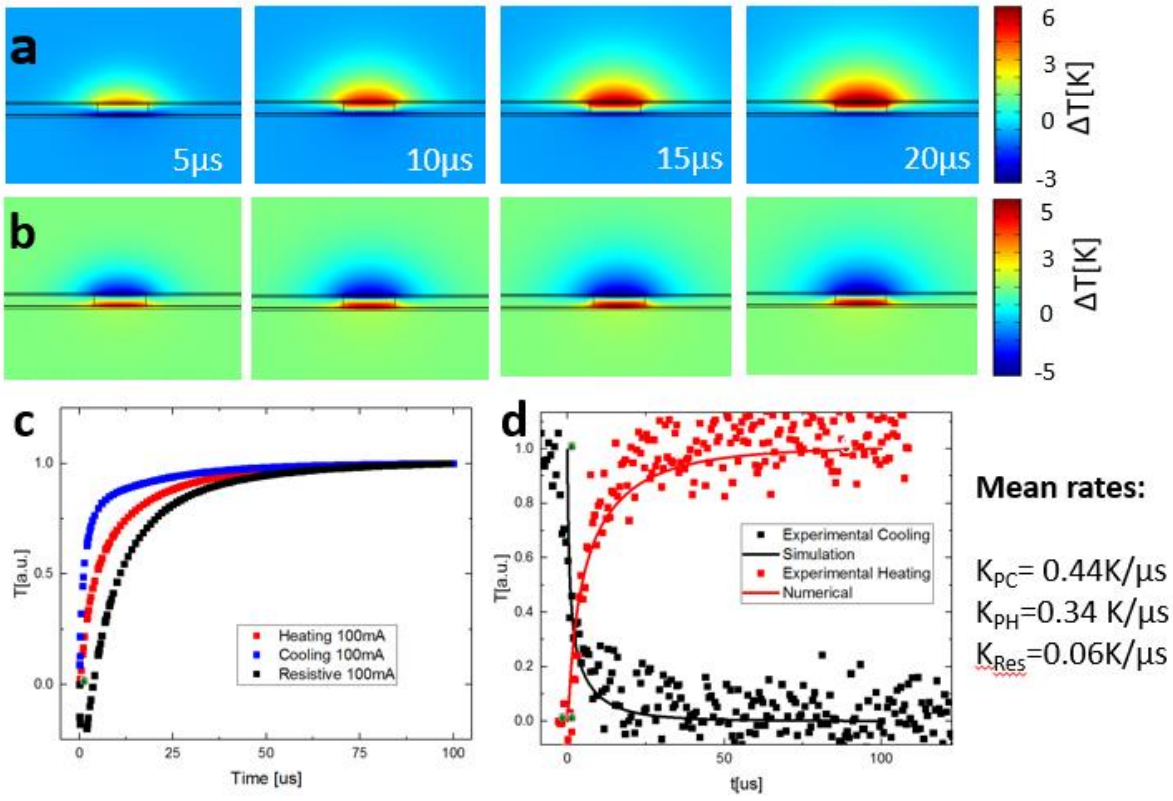


Figure 6. Device Time Response. FEM simulations in the time domain showing evolution of temperature **(a)** in heating mode **(b)** in cooling mode. **(c)** Simulated normalised time response of the average top contact temperature used to extract mean rates of temperature change. **(d)** Simulated results directly overlaid experimental measurements from thermoreflectance.

increases linearly with the diameter of the pads as shown in Supplemental Figure S3, where the time response was measured using a frequency domain technique.

Cooling Performance under applied heat load:

The cooling performance of this device was studied under an applied heat load by heating the surface using a laser. The incident laser was chopped to create a periodic heat source. A source current was triggered, simultaneously and with the same periodicity, such as to actively cool the top surface. The magnitude of the current was then swept to find a balancing point when the temperature rise on the pad goes to zero. Fig. 7c shows the temperature rise of the pad under laser

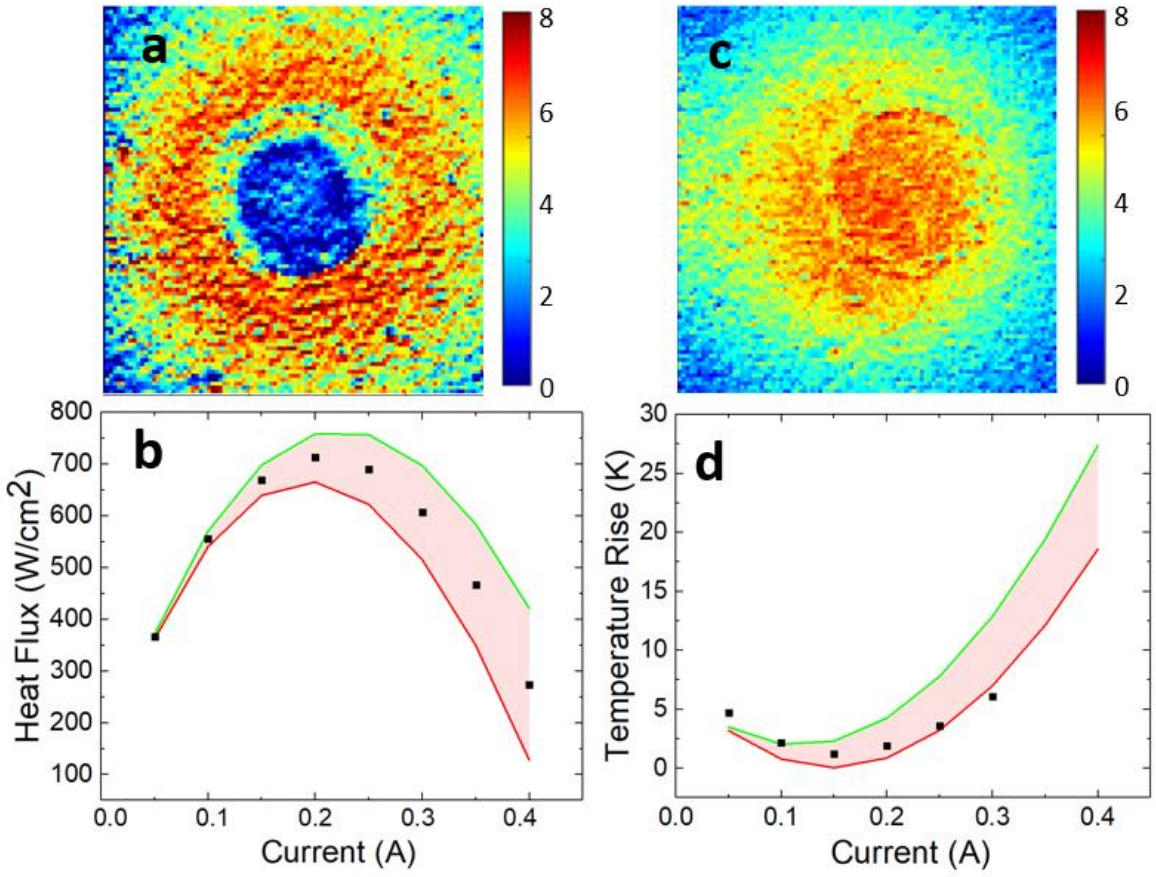


Figure 7 Device performance with heat load. (a) Temperature map with 8 mW incident on 22 μm pad pad and 150 mA cooling current applied. **(b)** The theoretical heat flux away from the top surface of the device for the 8 mW sweep **(c)** Temperature map with 8 mW incident on 22 μm diameter pad without cooling. **(d)** Mean net temperature achieved with 8 mW incident for the various cooling currents.

illumination without any active cooling. Fig. 7a shows the surface temperature when the cooling current is matched to produce zero temperature rise on the pad surface. The average pad temperature is compared to that expected from FEM simulations in Fig. 7c using the high and low values of thermal conductivity measured. From this we can extract the cooling heat flux as shown in Fig. 7d. As expected, there is an optimum current (200mA), which produces the highest cooling heat flux (720 ± 60 Wcm^{-2}). The coefficient of performance (COP) at this operational point was determined from the ratio of the cooling heat through the top central circular region to the power needed to produce this, with a COP of 0.26, which would be put this device as top of its electrodeposited for this length scale[39]. We note that the current heat flux performance is limited by our non-optimised device substrate. Further improvements in maximum heat flux are further possible by changing the device heat rejection characteristics. For example, using our experimentally validated numerical model, we predict a maximum heat flux of ~1 $kW.cm^{-2}$, an improvement of 32%, by changing the device substrate material to high quality diamond (see Fig. S6).

DISCUSSION

The performance of thin film thermoelectric materials and devices are difficult to measure accurately as small temperature differences across thin films must be quantified. In particular the main performance parameter ZT is sensitive to errors in the measurement of thermal conductivity, which is particularly difficult to measure accurately in thin films, and varies significantly depending on local morphology. In this work we have comprehensively measured electrical conductivity, electrical contact resistance, thermal conductivity, thermal contact resistance, and Seebeck coefficient locally using techniques with micron scale spatial resolution. This has allowed us to accurately measure the performance of an in situ micro-scale thermoelectric cooler and

demonstrate conclusively extreme heat flux handling capabilities surpassing state of the art for electrodeposited materials.

We have demonstrated devices which can achieve max cooling ΔT of -4.4 K under zero load, and have a response time of 20 μs, which is state of the art for electrodeposited devices in this size range. Furthermore, we characterised the performance of these devices under a simulated heat load by using a laser to heat the top surface. This demonstrated that we can dissipate maximum heat flux at zero temperature differential of 720 ± 60 Wcm^{-2} on our non-optimised substrate. By carefully designing the top contacts we were able to significantly reduce electrical contact resistance compared to other electrodeposited devices. This allowed us to make thinner devices than previously reported and still achieve net cooling increasing our critical heat flux. We demonstrated that passivation of the device with Si_3N_4, Ar-ion cleaning of the interface and the use of Tungsten as a top contact material significantly improves the performance and stability of the device.

The material ZT was calculated from direct measurements of electrical conductivity, thermal conductivity and Seebeck coefficient to be ZT=0.26 ($\pm$0.04). For a device zT, we can use the total thermal and electrical conductance's which include contact and interfacial values. This measured device zT then varies between 0.14, 0.24 and 0.26 for contact resistances of $10^{-10}/10^{-11}/10^{-12}$ Ωm^2. This is a reasonable value of ZT for an n-type Bi_2Te_3 electrodeposited sample, with ZT's ranging from 0.05 [39]-0.1 [33] all the way to 0.45 [32] with various lengths, although it should be noted that the higher value did not include a direct measurement of the thermal conductivity. Due to the difficulty in measuring the thermal conductivity accurately in thin films many groups forego this characterisation step, preferring instead to state the power factor of their material. The next highest

ZT found was 0.16 [34] putting our material ahead as the highest directly measured ZT for an undoped electrodeposited Bi_2Te_3 sample.

We claim that our measured critical heat flux of 720 $\pm$ 60 Wcm^{-2} is the largest recorded for electrodeposited thin film thermoelectric and the highest measured at room temperature. Again, due to the scarcity of thermal conductivity values necessary to model accurately a thin film device, and the difficulty in experimental procedure, there are not many directly measured examples to compare this to in the literature. Previous heat fluxes found for thin film thermoelectric devices range from 6.8 Wcm^{-2} for an electrodeposited BiTeSe film [39] to a record 1300 Wcm^{-2} for multilayer MOCVD devices [41], both of these values are predicted heat fluxes from simulations of the devices, with the former not using experimentally measured conductivities. The highest experimentally measured value[29] was 258 Wcm^{-2}. The above value of 1300 Wcm^{-2} was from heat generated from a resistive heater network which the TEC cooled by 7ºC, although this heater kept the device and substrate at 100ºC. Increasing the temperature of the measurement will generally increase the Seebeck coefficient and hence the max heat flux. If our measurement was taken at 100ºC with a small 10% increase in the Seebeck coefficient the heat flux would be expected to increase to 1400 Wcm^{-2}. From our simulations we expect that by optimising our geometry and material base could push the heat flux to > 1000 Wcm^{-2} at room temperature with a relatively inexpensive CMOS compatible fabrication process. Preliminary simulations as seen in Figure S5, show that the replacement of the low thermal conductivity oxide layer with a diamond interface would push the heat flux capacity to 1000 Wcm^{-2}. Future work will focus on demonstrating critical heat flux >1k Wcm^{-2} and integrating these cooling structures with real electronic and photonic devices.

CONCLUSIONS

In this work we present an electrodeposited TEC capable of pumping a maximum heat flux of 720 Wcm^{-2} at zero temperature difference. The device can maintain a temperature difference of 4.4 K under minimal heat load. All the relevant thermoelectric parameters were measured such as the Seebeck coefficient, electrical conductivity, thermal conductivity and heat flux yielding a ZT of 0.26. The heat flux stems from the thinness of the TEC, the functionality of which is normally limited by contact resistance. An electrical contact resistance $\sim 10^{-11}$ Ωm^2 was experimentally measured. This device also showed fast thermal time responses, with an experimentally measured $\tau = 20$ μs. Future work will focus on advancing the heat flux capabilities of these electrodeposited devices through modification of the back substrate material.

METHODS:

Electrodeposition.

A Ti (20 nm)/Au (100 nm) layer is sputtered on Si/SiO_2 substrate, which acts as a working electrode for electrodeposition of thin films using a three electrode set-up. A platinized titanium mesh and Ag/AgCl are used as the counter and the reference electrode, respectively. The electrolytic bath is prepared by dissolving precursor salts in 1 M HNO_3 acid solution. First 15 mM Te powder (Sigma Aldrich) is dissolved in 1 M HNO_3 solution at 40 $^{\circ}C$ under constant stirring. After the Te powder is fully dissolved giving a clear solution, 10 mM $Bi(NO_3)_3.5H_2O$ (Sigma Aldrich) was added to the solution and waited till it gets completely dissolved. The Bi_2Te_3 thin film is then deposited at -50 mV at a rate of about 1.0 μm hr^{-1} to a thickness of about 5.5 μm.

Contact deposition.

The top and bottom metal contact are evaporated using a Temescal FC2000 e-beam evaporation system. The process chamber is evacuated to $< 5\times10^{-7}$ Torr prior to evaporation. Bi_2Te_3 thin film

surface is treated with an Ar-ion etch in the chamber. During the process, the pressure of the chamber increased to 1×10^{-4} Torr. After that the ion chamber is evacuated to $< 5\times10^{-7}$ Torr. The metal is deposited at a rate of 0.3 nm s^{-1} to a thickness of 100 nm.

Frequency domain thermoreflectance.

Our custom FDTR setup is based on a pump and probe system. Built around two single mode continuous CW diode lasers with maximum output power of 120 mW. The pump laser wavelength is 403 nm, a wavelength which maximise absorbed power for Au, and the probe wavelength is 511 nm, which maximise the thermoreflectance signal from Au interface [42]. The Au contact pad acts as a transducer, and a lock-in amplifier is used to modulate the pump laser to provide localised heating and to record the amplitude and phase response of the reflected probe beam [43].

The uncertainty of our FDTR measurements is determined by a conservative but robust Monte Carlo method[44]. We fitted the data over 1000 iterations with varying input parameters to obtain the unknown variables distribution. The input variation accounted the margin of error for each of the controlled parameters by using a normal distribution with a defined range in the simulations. We then fitted each of the unknown variable distribution with lognormal fit and determined the 95% lower and upper confidence bounds.

CCD based thermoreflectance imaging.

In CCD bases thermoreflectance (CCD-TR) a periodic current source is applied to the device which in turn generates an oscillating temperature at the surface of the device. By triggering the CCD camera frame rate to a multiple of the current frequency we can obtain a series of images of the device when it is hot and cold. Taking the difference of the hot and cold images allows us to extract the change in reflectivity of the surface. The thermoreflectance coefficient of gold is quite

small (measured at -2.4×10^{-4} [K^{-1}]). Therefore, in order to obtain an image with good signal to noise we must average over a large number of frames. In our case we found that we could get acceptable temperature resolution of 0.125 K after 40,000 images. With a frame rate of 100 Hz this meant a single temperature map would take 3 minutes. The performance of the device was stable over this time, with consistent results being achieved even after 24 hours of continuous bipolar cycling. This equates to around 350,000 temperature cycles. Supplemental figure S4 shows how a laser was coupled into the standard CCD-TR setup. The measured time response of the device assured us that we are measuring the steady state temperature using this technique.

Finite Element method simulations.

Finite element modelling was carried using COMSOL Multiphysics, coupling electrostatic and thermal modules. This implements coupling between the heat equation and the current density modified with the thermoelectric equations such that the current density becomes $\boldsymbol{J} = \sigma(-\nabla V - S\nabla T)$ and an additional Peltier contribution, $\dot{\boldsymbol{q}} = P\boldsymbol{J}$, is added to the heat flux on boundaries . No temperature dependencies of the thermoelectric parameters were introduced, and as such the Thomson effect wasn't modelled. Taking the temperature dependence of the Seebeck coefficient of bulk bismuth telluride and a ΔT of 4.4 K, the expected contribution of the Thomson effect relative to the other thermoelectric effects is <1% at a current of 200mA. This relative contribution will increase with higher temperature gradients at lower currents. This constant property model is assumed to be the cause of the discrepancy between the model and experimental results at higher temperatures such as in Figures 1.c, 5.c. However, this effect can be assumed to be negligible for the measurement of the max cooling heat flux in Figure 7 due to low temperature difference across the TE material. The full device structure as shown Fig. 1a was designed in a 2D axisymmetric model using the material properties outlined in Table S1. Physics controlled mesh densities were

used such that vertical mesh densities were roughly 1 domain/ 100nm near to the metal layers and reaching a maximum of 3 domains/μm in the centre of the TE material. The total number of domains was approximately 61,000 with a total of 250,000 DOF. To model the experimental cases where the laser is used to optically heat the top surface, an equivalent circular uniform boundary heat source is introduced on the top contact. This heat flux is corrected for losses through the microscope setup and the measured absorption of 488nm light on the Au circular pads.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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Supporting Information

Table S1. Parameters used for FEM simulations. Figure S1 Optical images showing various metal contacts and their diffusion into the TE layer. Figure S2. The effect of contact resistance on the top pad temperature. Figure S3. Time constant of cooling for various pad diameters. Figure S4 Optical pathway for the laser induced heating and CCD-TR setup. Figure S5 Effect of alternative back substrate. Figure S6 FEM meshing of model and temperature gradients across device.

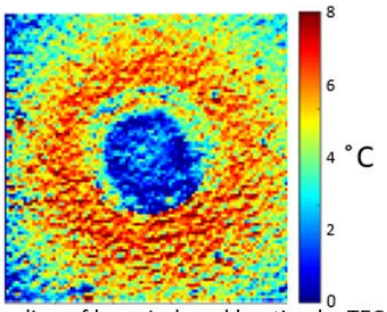
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529 For Table of Contents Only



530 Cooling of laser induced heating by TEC